

MODEL NAME : VAW01
PROJECT CODE : ANRVAW0100
PCB NO : LA-9101P (Mars Pro)

DA60000UT00 LA-9101P M/B
DA40001FO00 LS-9101P POWER BUTTON/B
DA40001FP00 LS-9102P USB/B
DA40001FQ00 LS-9103P TP BUTTON/B

ZZZ R1@
PCB VAW01 LA-9101P LS-9101P/9102P/9103P
DAZ0U500100

ZZZ GCER3@
PCB VAW01 LA-9101P LS-9101P/9102P/9103P GOLD A31 !
DAZ0U500101

ZZZ TRIR3@
PCB VAW00 LA-9101P LS-9101P/9102P/9103P TRIPOD A31 !
DAZ0U500102

ZZZ HANNR3@
PCB VAW00 LA-9101P LS-9101P/9102P/9103P HANNSTARB A31 !
DAZ0U500103

ZZZ ZDTR3@
PCB VAW00 LA-9101P LS-9101P/9102P/9103P ZDT A31 !
DAZ0U500104

Dell / Compal Confidential

Schematic Document

Intel Chief River

Ivy Bridge (BGA) + Panther Point

OAK 15" UMA/DIS AMD Mars Pro

2012-08-22

Rev: 0.4

46@ : for 46 level
@ : Nopop Component
CONN@ : Connector Component
KB9012@ : ENE KB9012 Implemented
UMA@ : Only for UMA
EMC@ : EMI/ESD parts

R1@ : R1 P/N
R3@ : R3 P/N

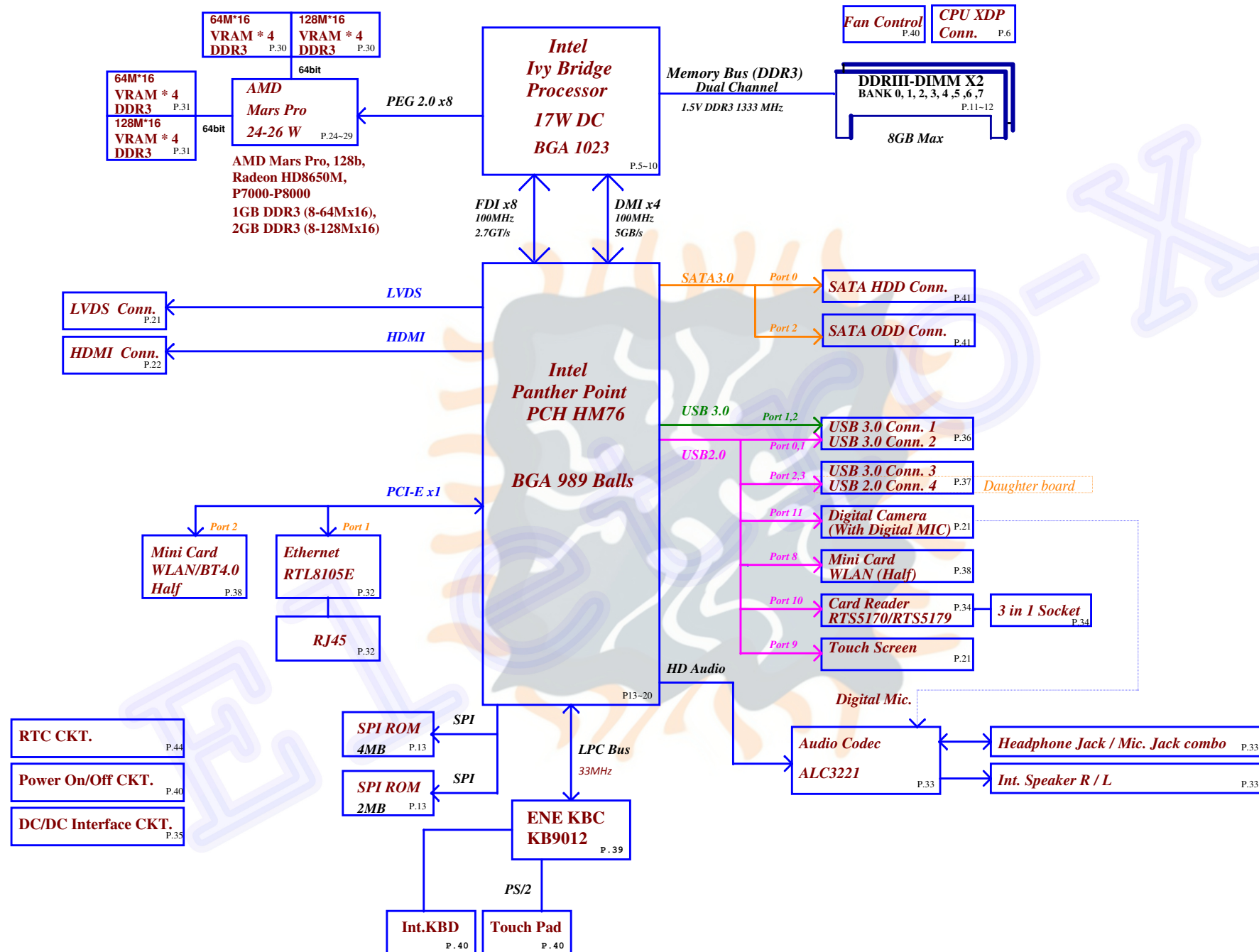
i3R1@ : CPU i3-3217 1.8G
i3VOSR1@ : CPU i3-2365 1.4G
i5R1@ : CPU i5-3317 1.7G
i7R1@ : CPU i7-3517 1.9G
CEL1@ : CPU Celeron 887 1.5G
PENR1@ : CPU Pentium 997 1.6G

DIS@ : Only for Discrete
TH@/THR1@ : Thames-XT
MS@/MSR1@ : Mars Pro
X76@ :
SPI-ROM & VRAM Group

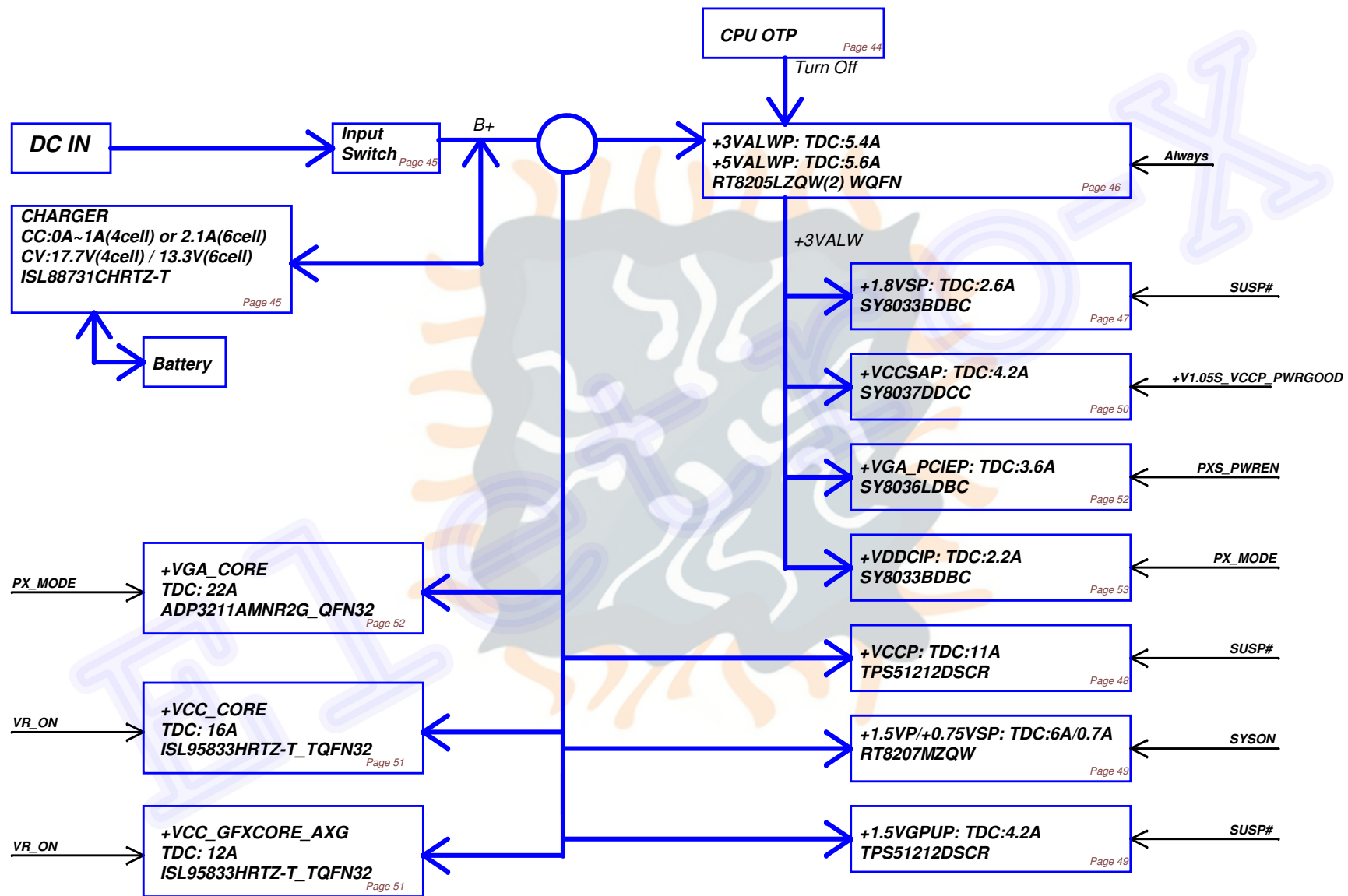
GCLK@ : Green CLK implemented
GCLKUMA@ : Green CLK for UMA
GCLKDIS@ : Green CLK for DIS
XTAL@ : X'tal implemented

XTALDIS@ : X'tal with DIS implemented

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/08/22	Deciphered Date	2013/08/31	Title Cover Page
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number LA-9101P
				Date: Wednesday, August 28, 2012 Sheet 1 of 57

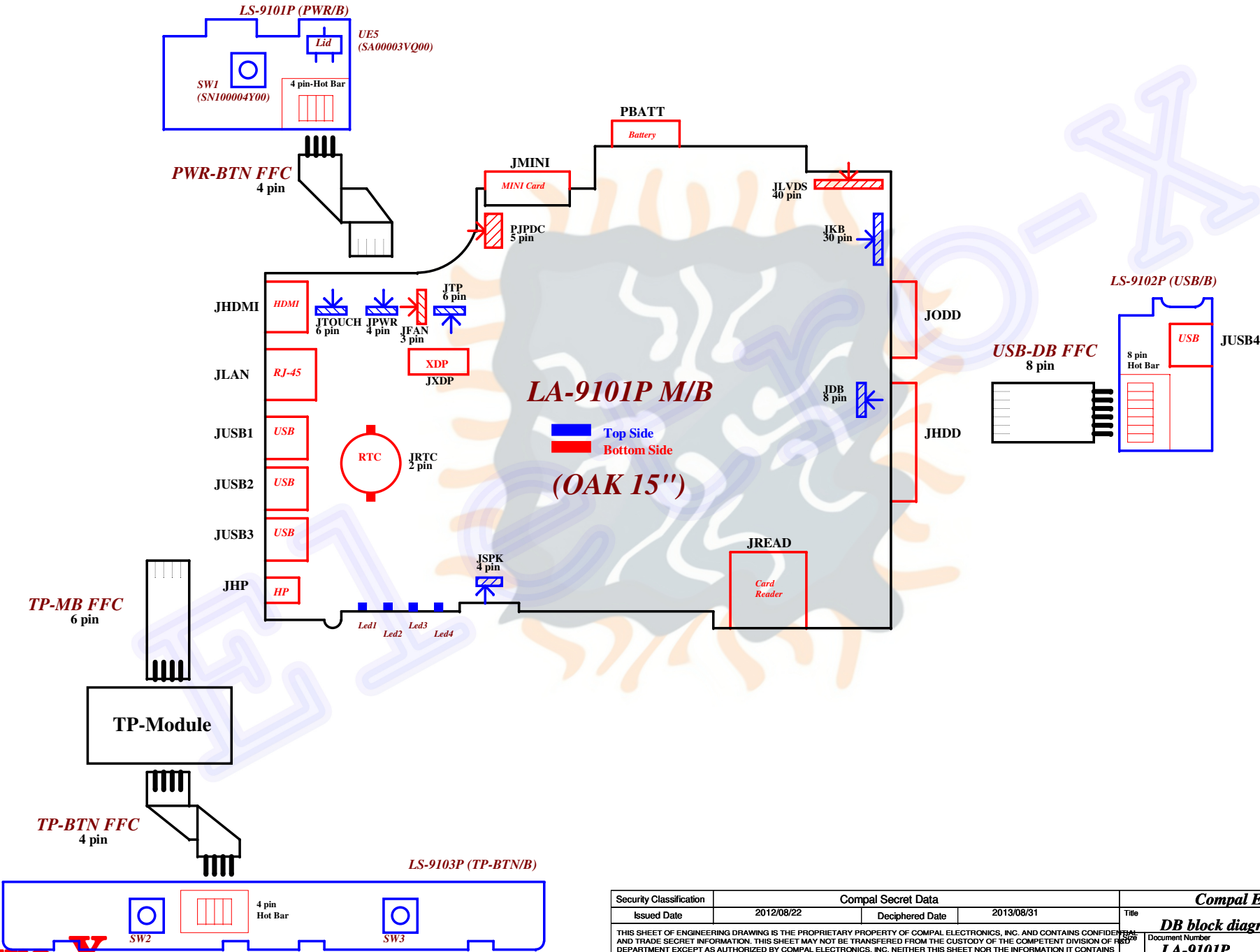


Power block



Compal Confidential

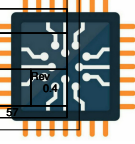
Project Code : VAW01
File Name : LA-9101P



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF HEADQUARTERS WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			

Compal Electronics, Inc.	
Title	DB block diagram
Document Number	LA-9101P
Date	Wednesday, August 29, 2012
Sheet	3 of 5

Eleetro-X



Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

ID	PCB Revision
0	0.1
1	0.1
2	0.2
3	0.2
4	0.3
5	0.4
6	1.0
7	1.0
UMA	THM
	MARS

Project ID Table

ID	Project Revision
0	
1	
2	
3	
4	
5	UMA
6	DIS THAMES
7	DIS MARS PRO

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	Express Card	Thermal Sensor	FFS	VGA Thermal Sensor	VGA	XDP	Charger
EC_SMB_CK1 EC_SMB_DA1	KB9012			V								V
EC_SMB_CK2 EC_SMB_DA2	KB9012								V	V		
PCH_SML0CLK PCH_SML0DATA	PCH											
PCH_SML1CLK PCH_SML1DATA	PCH											
MEM_SMBCLK MEM_SMBDATA	PCH	V	V		V	V		V			V	



PCH	USB PORT#	DESTINATION
	0	USB conn.2
	1	USB conn.1
	2	USB conn.3
	3	USB conn.4 (DB)
	4	NC
	5	NC
	6	NC
	7	NC
	8	MINI CARD (WLAN)
	9	Touch Screen
	10	Card Reader
	11	Camera
	12	NC
	13	NC

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	10/100 LAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	MINI CARD WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	None	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

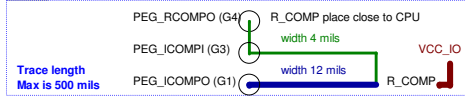
PCI EXPRESS	DESTINATION
Lane 1	10/100 LAN
Lane 2	MINI CARD (WLAN)
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

Symbol Note :

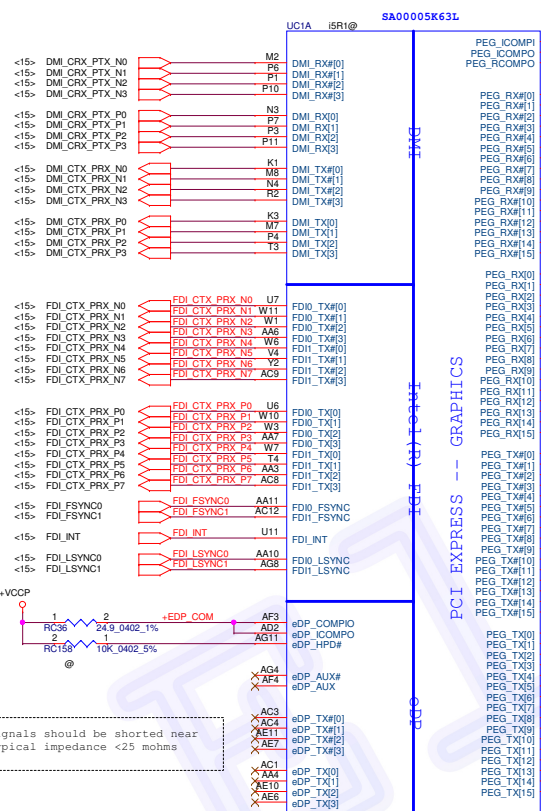




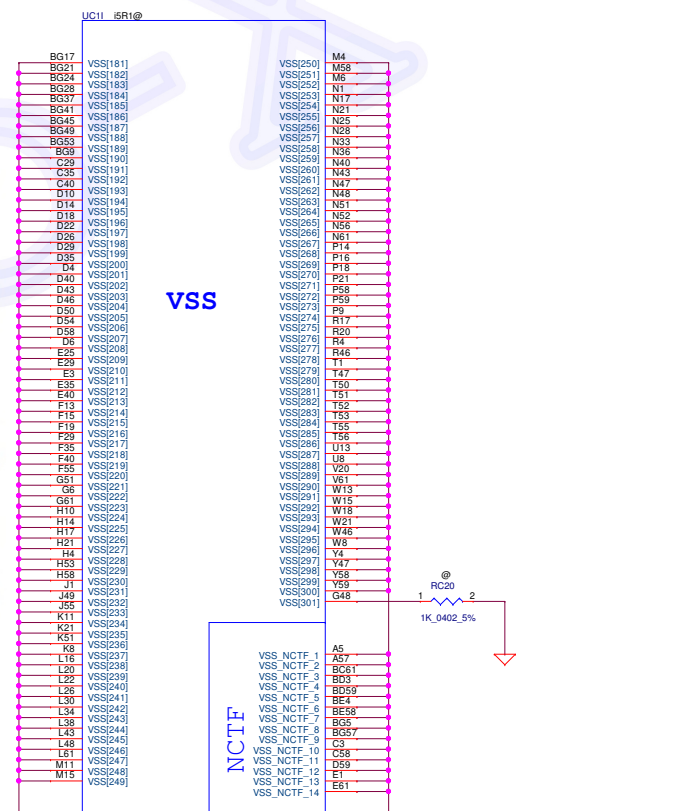
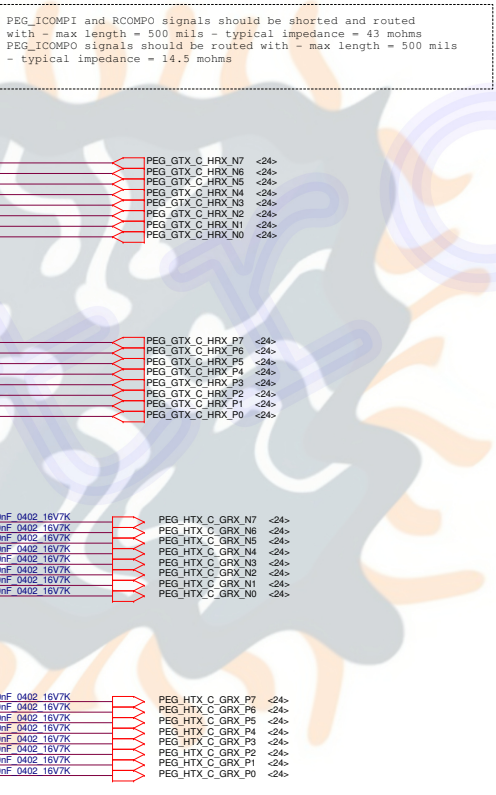
(1) PEG_RCOMP0 (G4) use 4mil connect to PEG_ICOMPI, then use 4mil connect to RC1.
(2) PEG_ICOMPI use 12mil connect to RC1

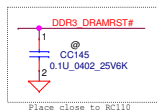
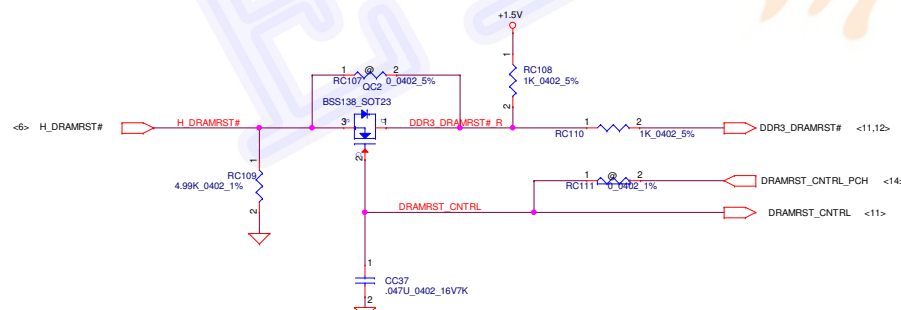
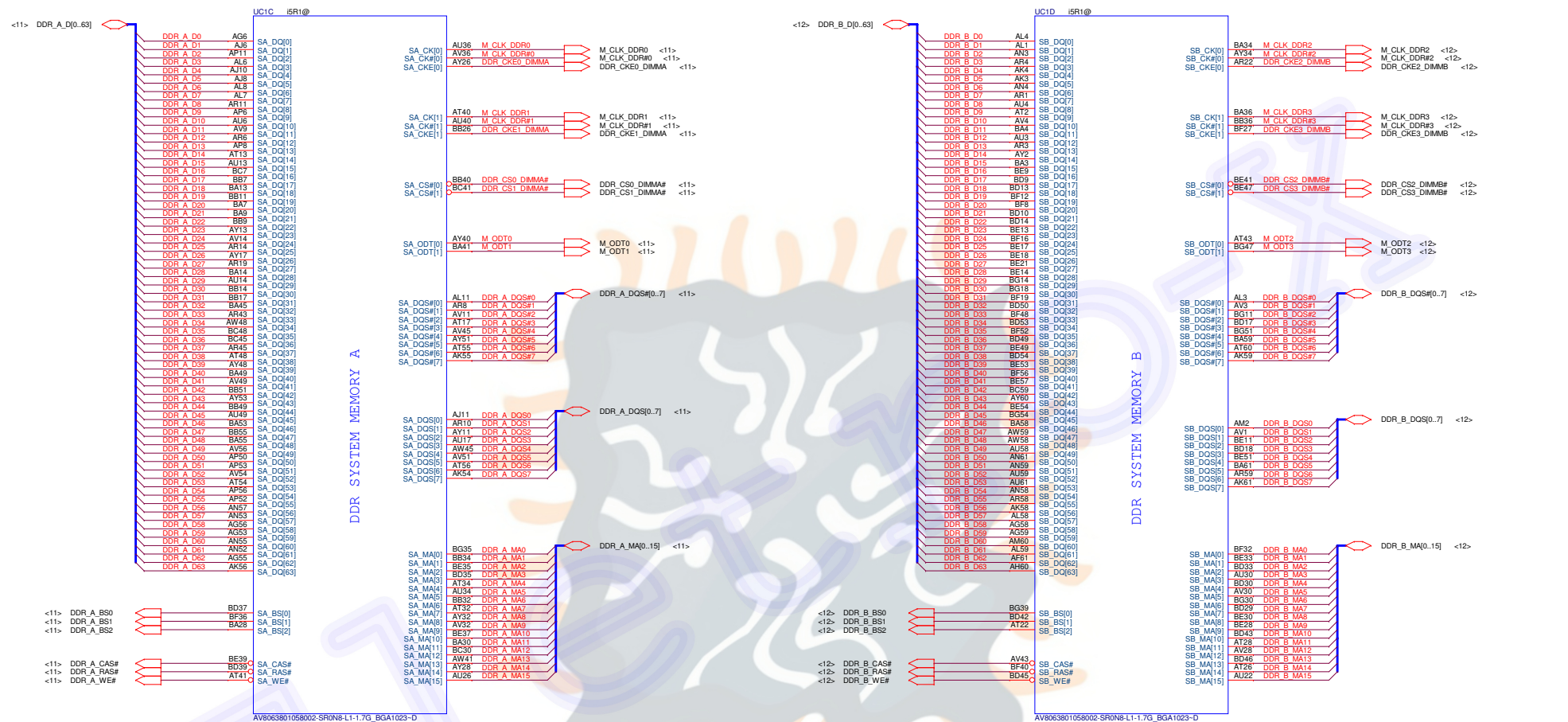


PEG_ICOMPI and RCOMP0 signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

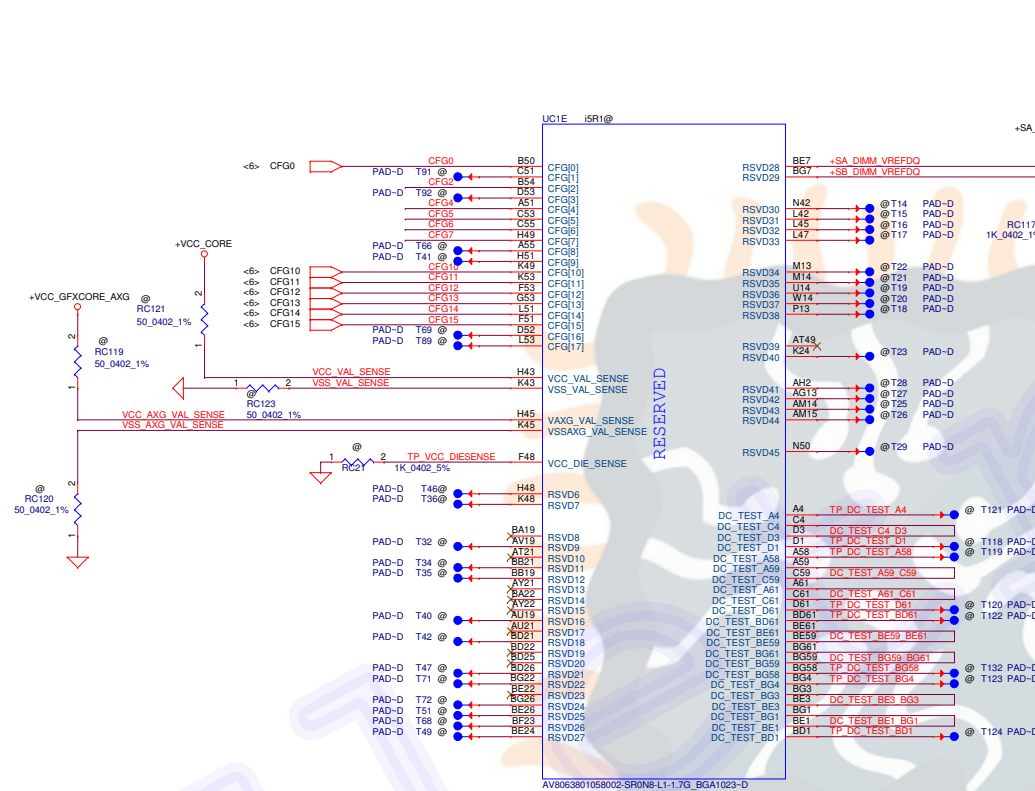


PCI EXPRESS -- GRAPHICS





CFG Straps for Processor



CFG2	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

CFG4	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

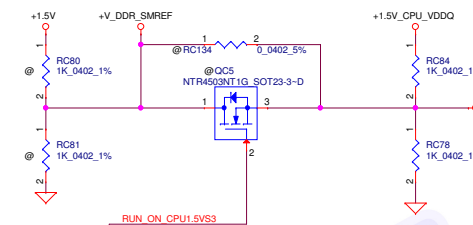
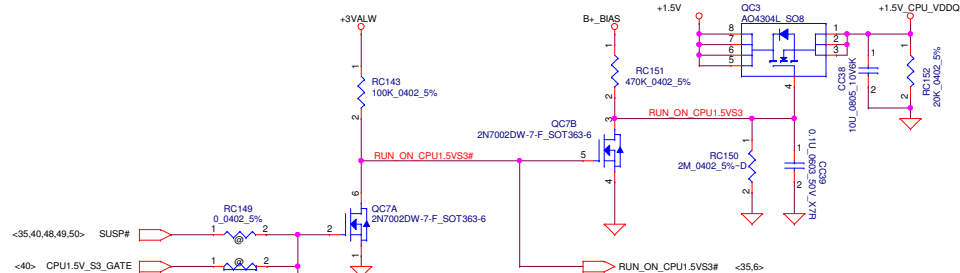
CFG[6:5]	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

CFG7	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

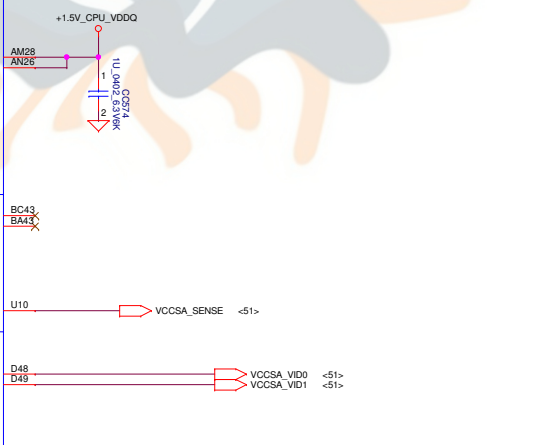
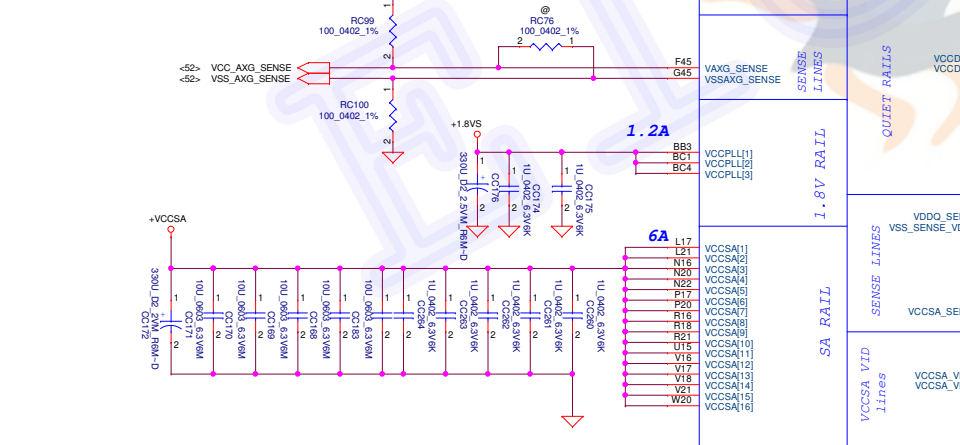
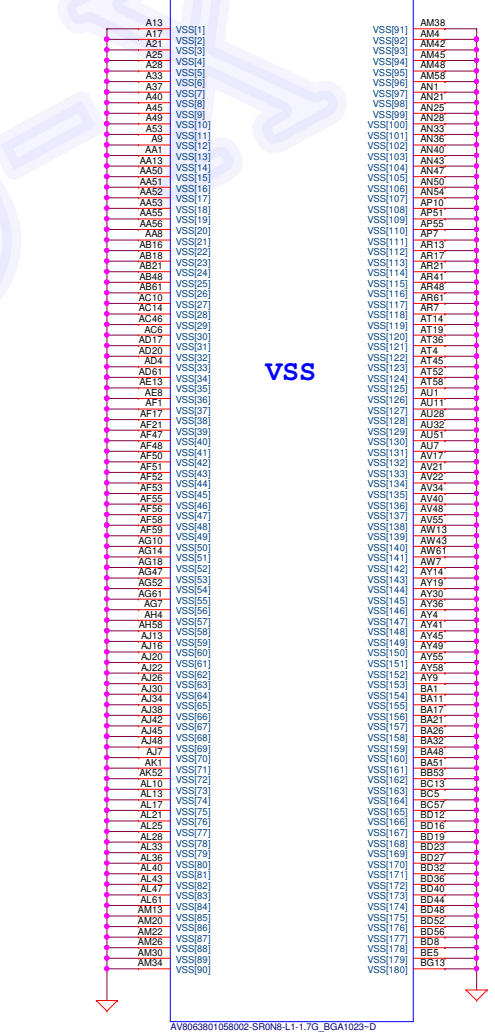
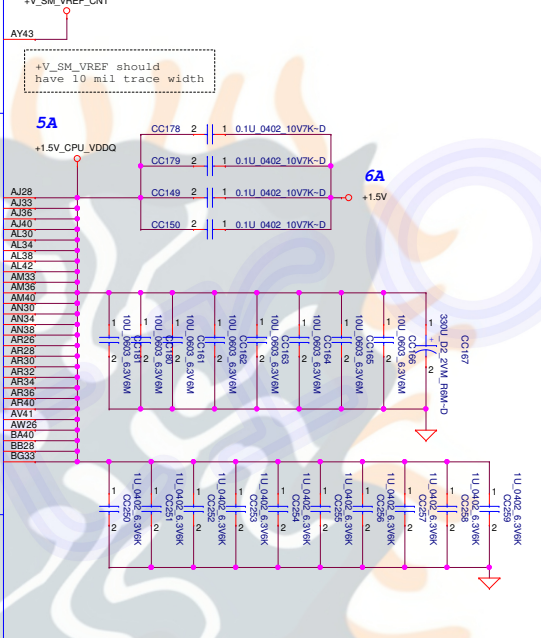
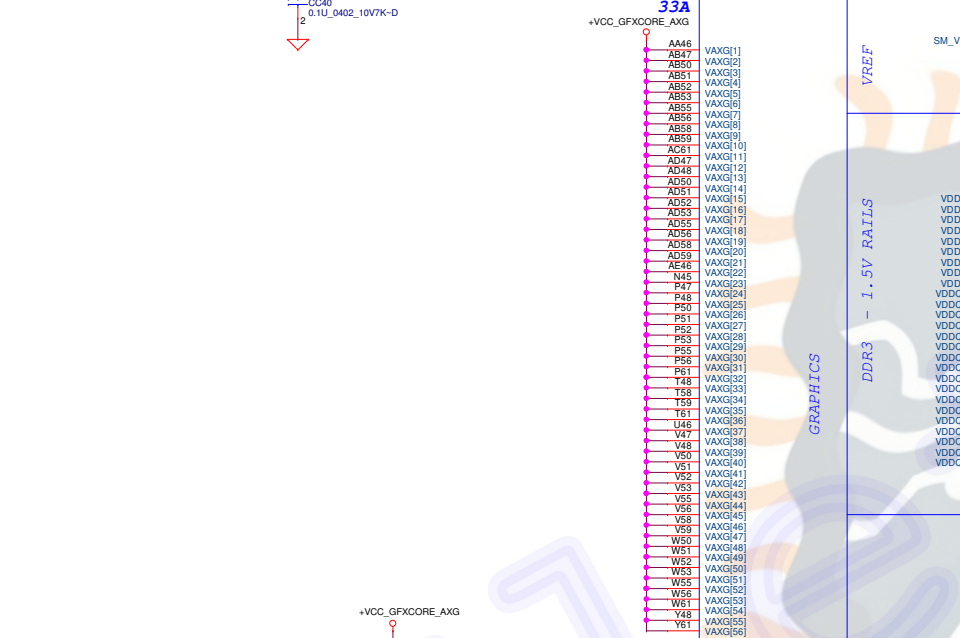


CPU Power Rail Table		
Voltage Rail	Voltage	50 Iccmax Current (A)
VCC	0.65-1.3	53
VCCIO	1.05/1	8.5
VauxG	0.0-1.1	33
VCCPLL	1.8	1.2
VDDQ	1.5	5
VCCSA	0.65-0.9	6
+1.5V_MEM	1.5	12-16
* Description 5A to Mem controller(+1.5V_CPU_VDDQ) 5-6A to 2 DIMMs/channel 2-5A to +1.5V_RUN & +0.75V_DDR_VTT		

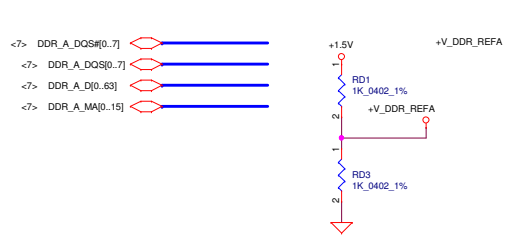
+1.5V_CPU_VDDQ Source



POWER

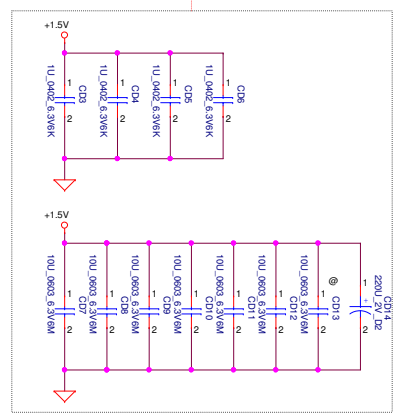


AV8063801058002-SRON8-L1-1.7G_BGA1023-D

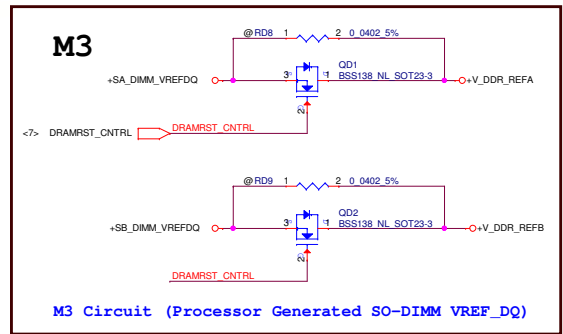
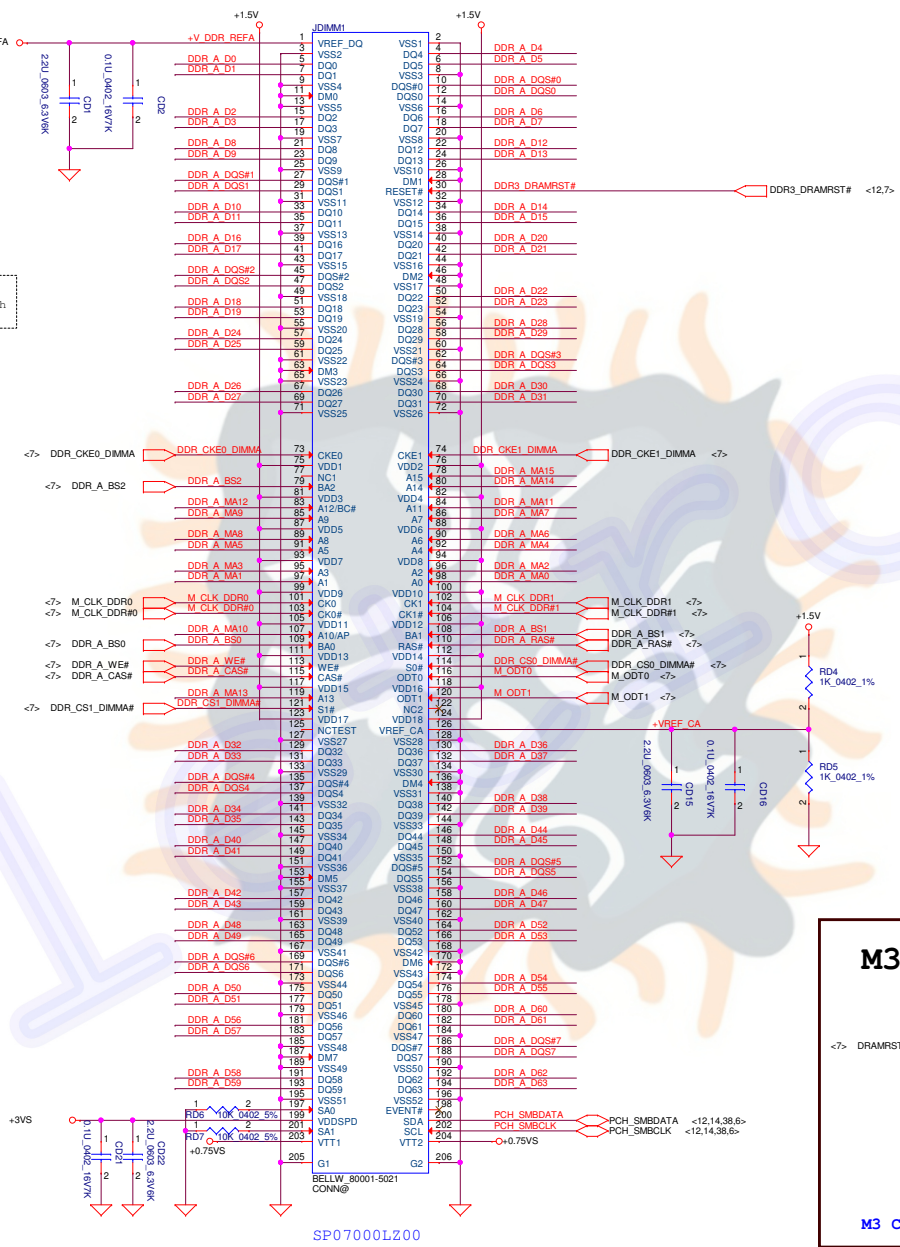
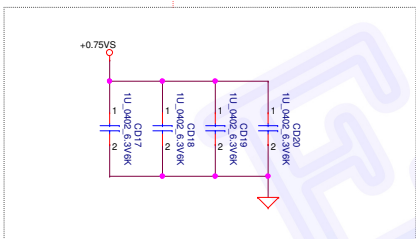


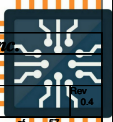
Layout Note:
Place near JDIMM1

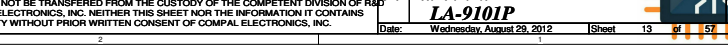
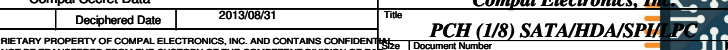
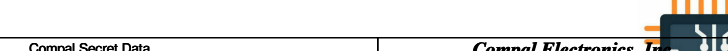
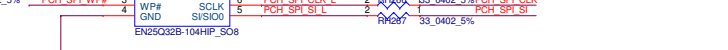
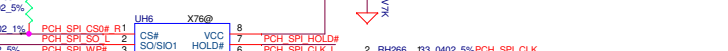
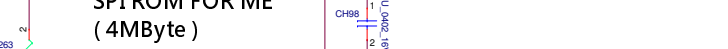
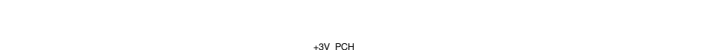
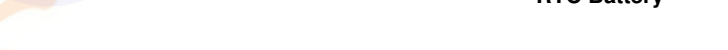
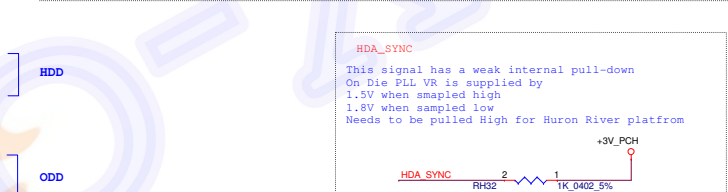
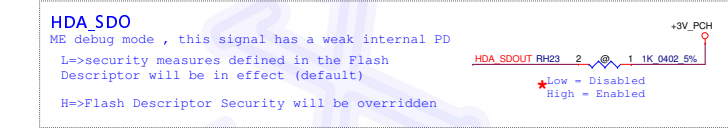
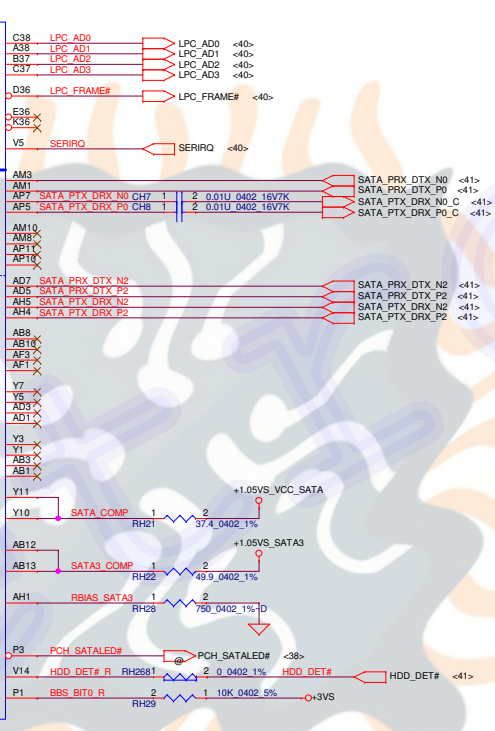
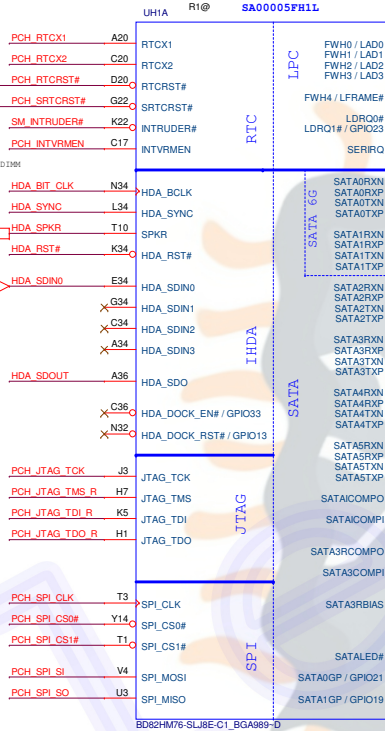
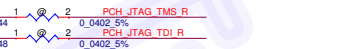
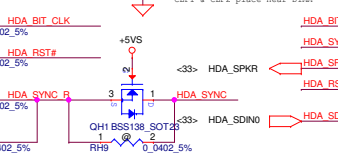
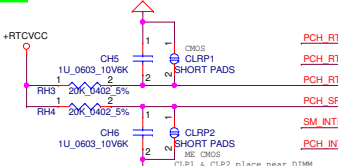
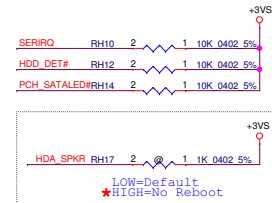
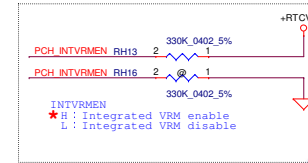
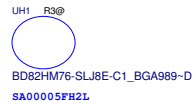
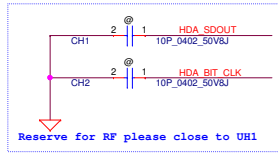
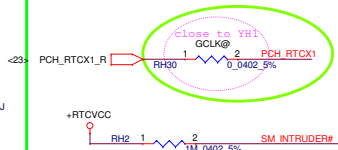
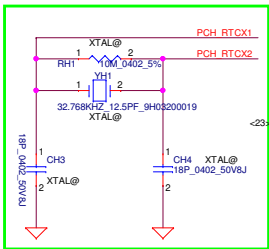
All VREF traces should have 10 mil trace width

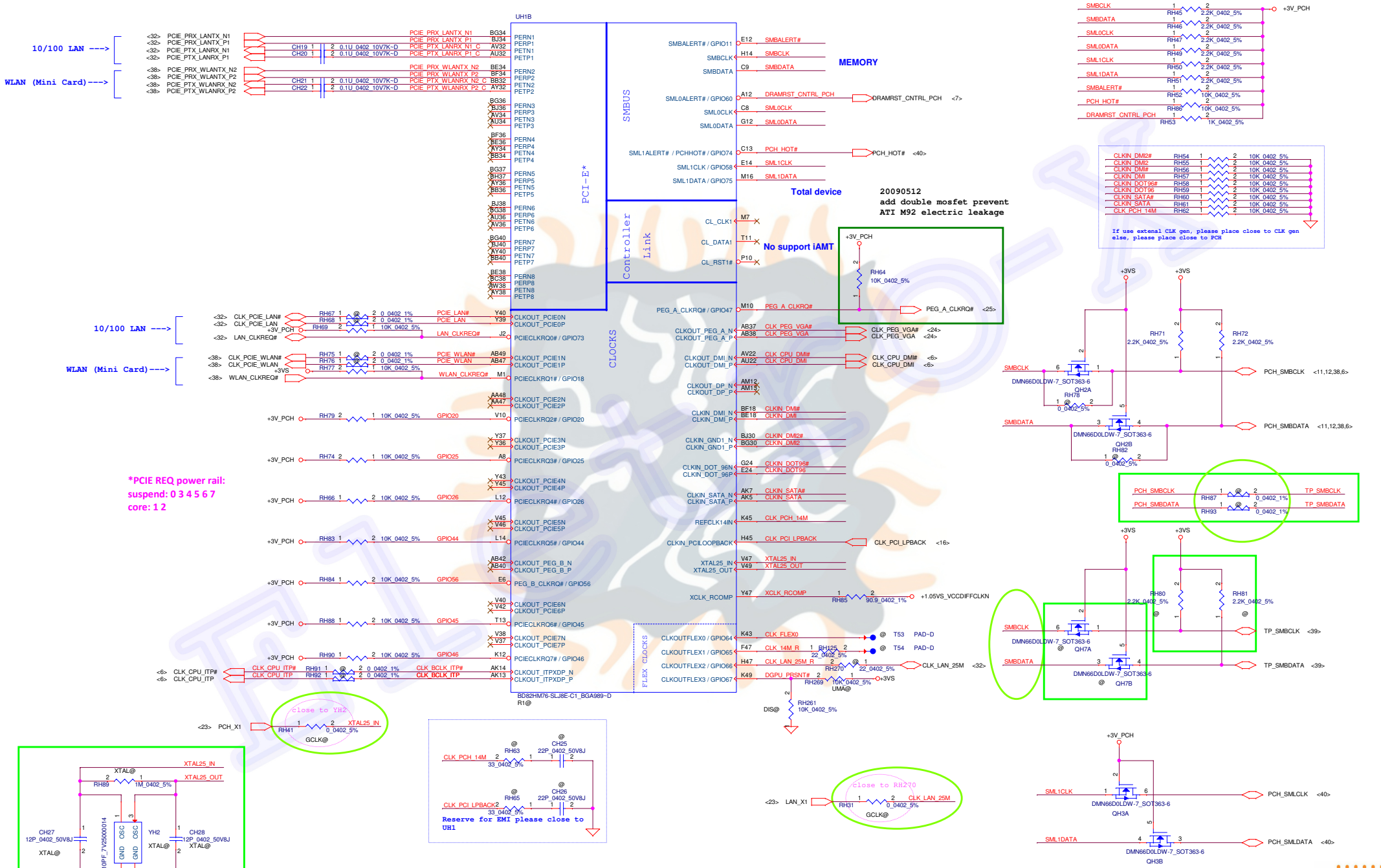


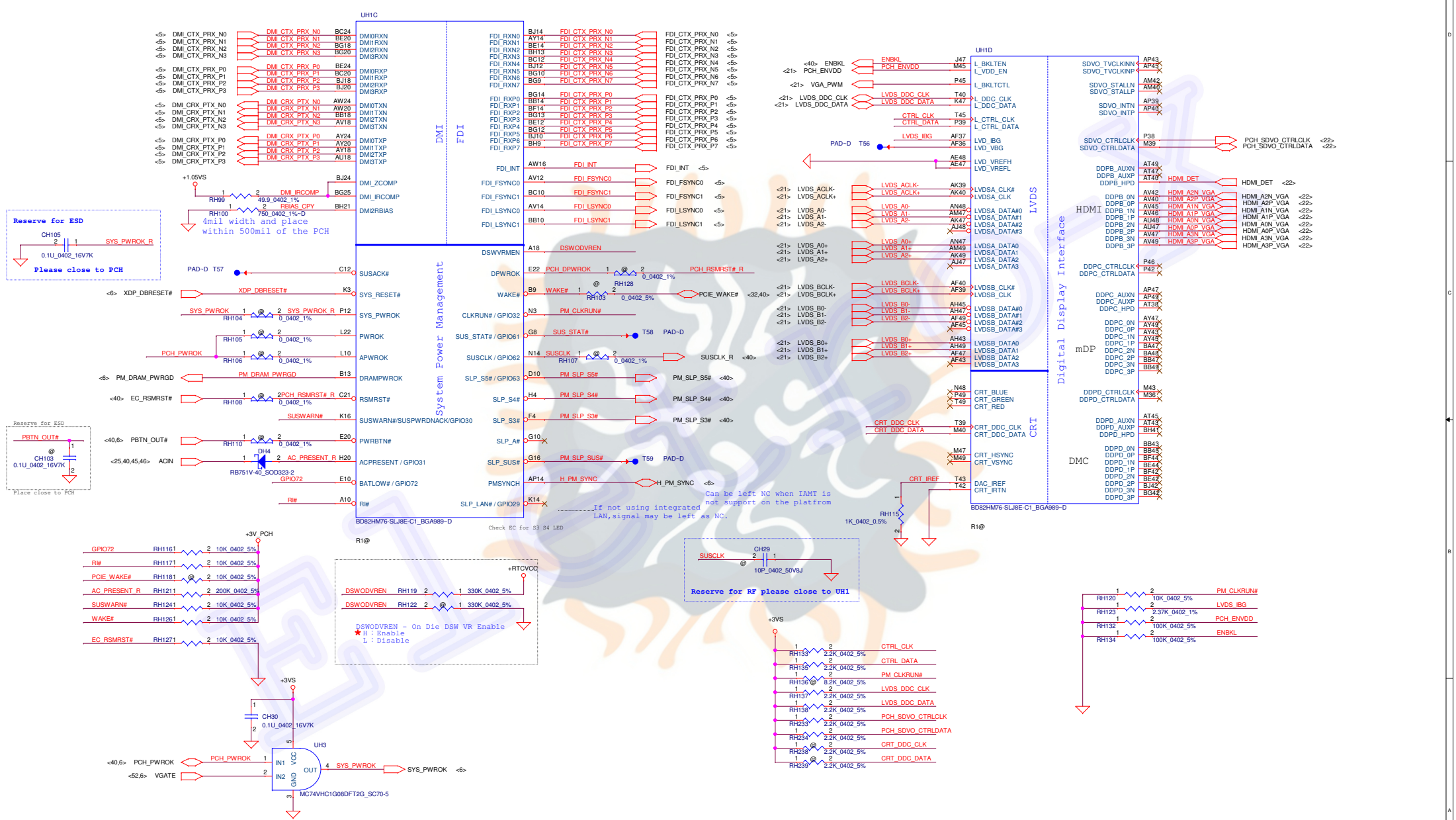
Layout Note:
Place near JDIMM1.203,204

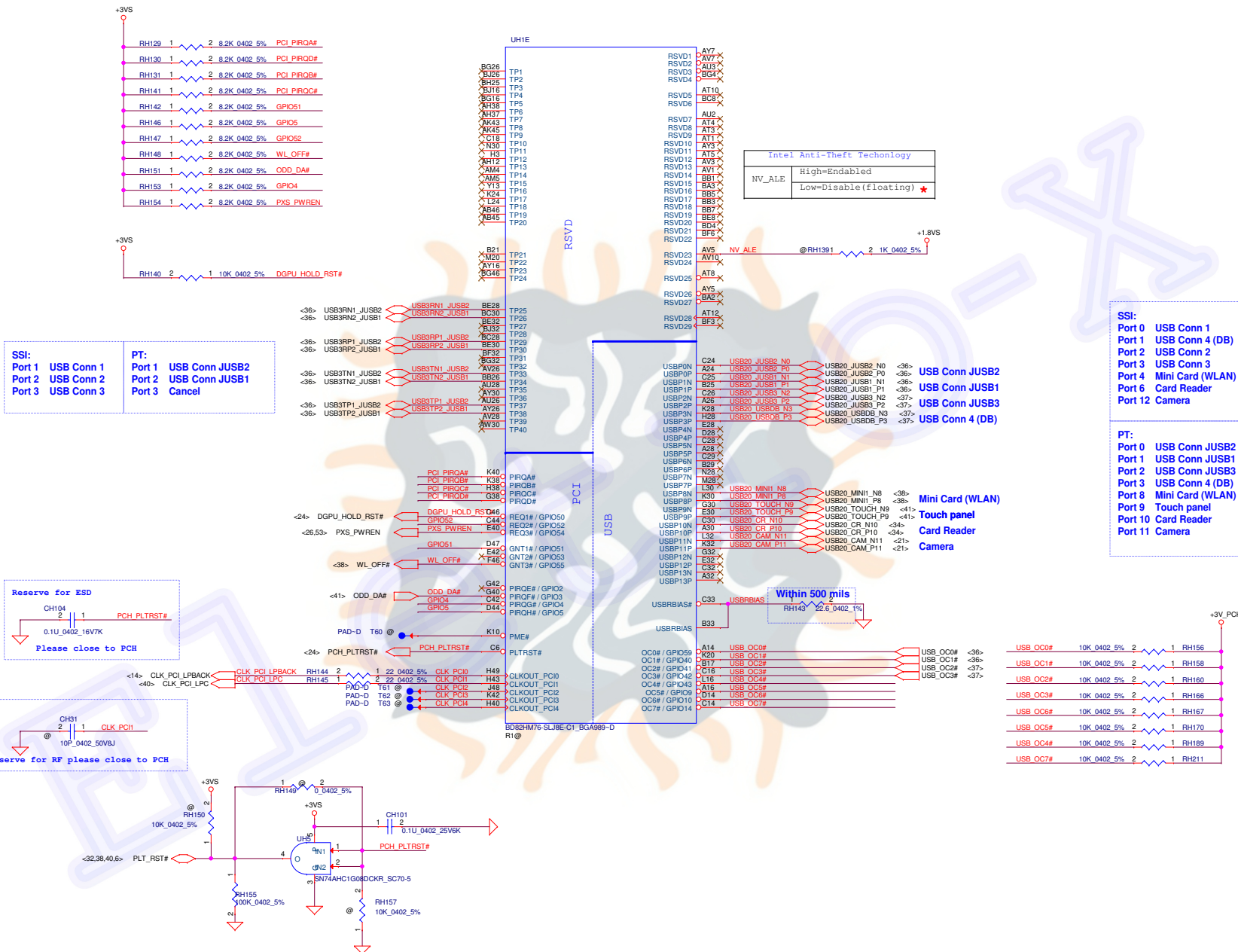




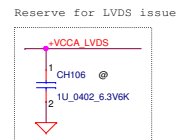












Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31
<p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RESEARCH AND DEVELOPMENT TO ANY OTHER DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT THE WRITTEN CONSENT OF THE COMPETENT DIVISION OF RESEARCH AND DEVELOPMENT. THIS SHEET MAY NOT BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM, WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</p>			

H5	VSS[0]	UH1H
AA17	VSS[11]	AK38
AA2	VSS[12]	AK4
AA3	VSS[13]	AK42
AA33	VSS[14]	AK46
AA34	VSS[15]	AK8
AB11	VSS[16]	AL16
AB14	VSS[17]	AL17
AB39	VSS[18]	AL19
AB4	VSS[19]	AL2
AB43	VSS[20]	AL21
AB5	VSS[21]	AL23
AB7	VSS[22]	AL28
AC19	VSS[23]	AL27
AC2	VSS[24]	AL31
AC21	VSS[25]	AL33
AC24	VSS[26]	AL34
AC33	VSS[27]	AL48
AC34	VSS[28]	AM11
AC48	VSS[29]	AM14
AD10	VSS[30]	AM36
AD11	VSS[31]	AM39
AD12	VSS[32]	AM43
AD13	VSS[33]	AM45
AD19	VSS[34]	AM46
AD24	VSS[35]	AM7
AD26	VSS[36]	AN2
AD27	VSS[37]	AN29
AD33	VSS[38]	AN3
AD34	VSS[39]	AN31
AD36	VSS[40]	AP12
AD37	VSS[41]	AP19
AD38	VSS[42]	AP28
AD39	VSS[43]	AP30
AD4	VSS[44]	AP32
AD40	VSS[45]	AP38
AD42	VSS[46]	AP4
AD43	VSS[47]	AP42
AD45	VSS[48]	AP46
AD46	VSS[49]	AP6
AD8	VSS[50]	AR2
AE2	VSS[51]	AR48
AE3	VSS[52]	AT11
AF10	VSS[53]	AT13
AF12	VSS[54]	AT18
AD14	VSS[55]	AT22
AD16	VSS[56]	AT26
AF16	VSS[57]	AT28
AF19	VSS[58]	AT30
AF24	VSS[59]	AT32
AF26	VSS[60]	AT34
AF27	VSS[61]	AT38
AF29	VSS[62]	AT42
AF31	VSS[63]	AT46
AF38	VSS[64]	AT7
AF4	VSS[65]	AU24
AF42	VSS[66]	AU30
AF46	VSS[67]	AV16
AF5	VSS[68]	AV20
AF7	VSS[69]	AV24
AF3	VSS[70]	AV30
AG19	VSS[71]	AV38
VSS[72]		AV4
AG31	VSS[73]	AV43
AG48	VSS[74]	AV8
AH11	VSS[75]	AW14
AH3	VSS[76]	AW15
AH36	VSS[77]	AW2
AH39	VSS[78]	AW22
AH40	VSS[79]	AW26
AH42	VSS[80]	AW28
AH46	VSS[81]	AW32
AH7	VSS[82]	AW34
AJ19	VSS[83]	AW38
AJ21	VSS[84]	AW40
AJ24	VSS[85]	AW48
AJ33	VSS[86]	AV11
AJ34	VSS[87]	AV12
AK12	VSS[88]	AV22
VSS[89]		AV28
AK3	VSS[90]	

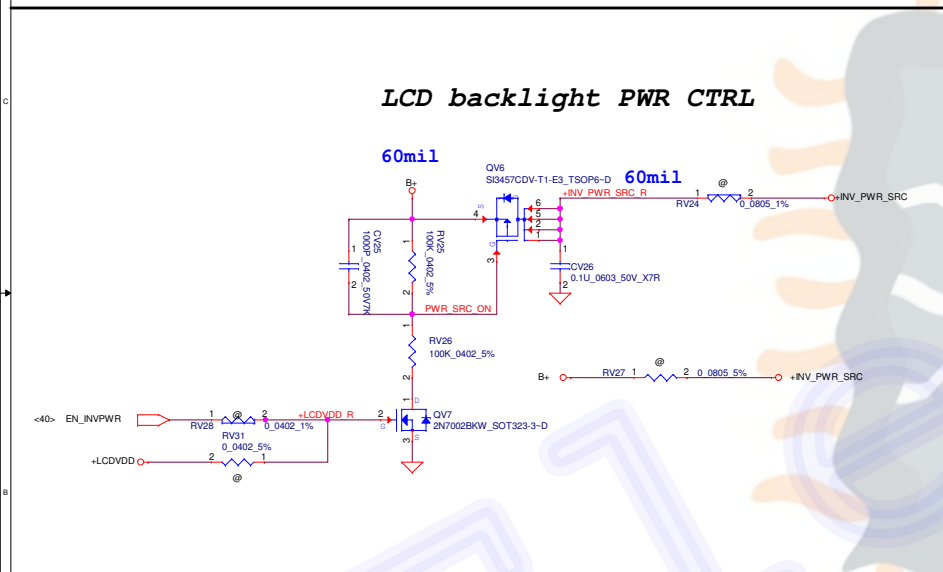
BD82HM76-SLJ8E-C1_BGA989-D

R1@

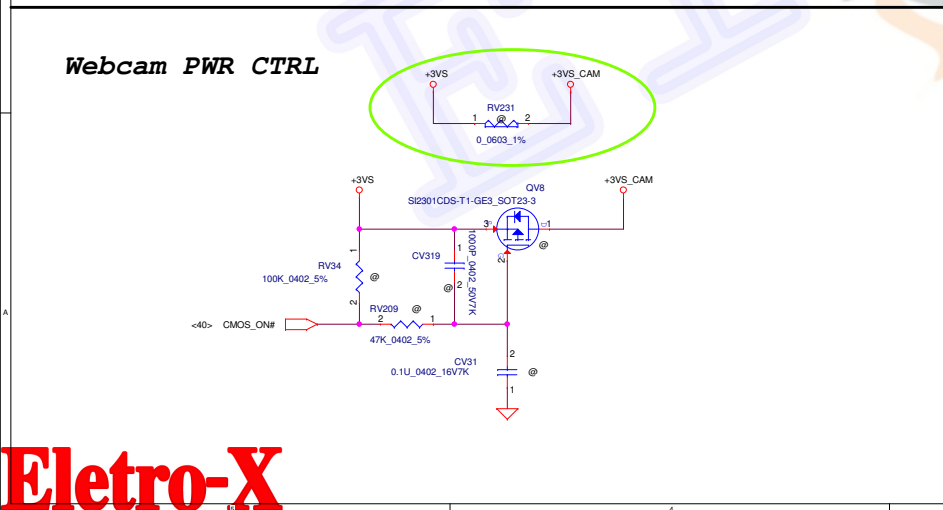
UH1	VSS[159]	H46
AY4	VSS[160]	K18
AY42	VSS[161]	K26
AY46	VSS[162]	K39
AY8	VSS[163]	K46
B11	VSS[164]	K7
B15	VSS[165]	L18
B19	VSS[166]	L2
B23	VSS[167]	L20
B27	VSS[168]	L26
B31	VSS[169]	L28
B35	VSS[170]	L36
B39	VSS[171]	L46
B7	VSS[172]	M12
F45	VSS[173]	M16
BB12	VSS[174]	M18
BB16	VSS[175]	M22
BB20	VSS[176]	M24
BB22	VSS[177]	M30
BB24	VSS[178]	M32
BB28	VSS[179]	M34
BB30	VSS[180]	M38
BB36	VSS[181]	M4
BB4	VSS[182]	M42
BB46	VSS[183]	M46
BC14	VSS[184]	M6
BC18	VSS[185]	M8
BC2	VSS[186]	M18
BC22	VSS[187]	M30
BC26	VSS[188]	N47
BC32	VSS[189]	P11
BC34	VSS[190]	P18
BC36	VSS[191]	T33
BC40	VSS[192]	P40
BC42	VSS[193]	P43
BC48	VSS[194]	P47
BD46	VSS[195]	P7
BQ5	VSS[196]	R2
AP12	VSS[197]	R48
BE22	VSS[198]	T12
BE26	VSS[199]	T31
BF10	VSS[200]	T37
BF12	VSS[201]	T4
BF16	VSS[202]	W34
BF20	VSS[203]	T46
BF22	VSS[204]	T47
BF24	VSS[205]	T6
BF26	VSS[206]	V11
BF28	VSS[207]	V17
BF30	VSS[208]	V26
BF38	VSS[209]	V29
BF40	VSS[210]	V31
BF8	VSS[211]	V36
BG17	VSS[212]	V39
BG21	VSS[213]	V43
BG33	VSS[214]	V7
BG44	VSS[215]	W17
BH38	VSS[216]	W19
BH11	VSS[217]	W2
BH15	VSS[218]	W27
BH17	VSS[219]	W48
BH19	VSS[220]	Y12
H10	VSS[221]	Y38
BH27	VSS[222]	Y4
BH31	VSS[223]	Y42
BH33	VSS[224]	Y46
BH35	VSS[225]	Y6
BH39	VSS[226]	BC29
BH43	VSS[227]	N24
BH7	VSS[228]	A3
D3	VSS[229]	AD47
D12	VSS[230]	B43
D16	VSS[231]	BE10
D18	VSS[232]	BG41
D22	VSS[233]	G14
D24	VSS[234]	H16
D26	VSS[235]	T36
D30	VSS[236]	BC22
D32	VSS[237]	BC24
D34	VSS[238]	C22
D38	VSS[239]	AP13
D42	VSS[240]	M14
D8	VSS[241]	AP3
E18	VSS[242]	AP7
E26	VSS[243]	BC16
G18	VSS[244]	BC28
G20	VSS[245]	S28
G26	VSS[246]	
G28	VSS[247]	
G36	VSS[248]	
G48	VSS[249]	
H12	VSS[250]	
H18	VSS[251]	
H22	VSS[252]	
H24	VSS[253]	
H26	VSS[254]	
H30	VSS[255]	
H32	VSS[256]	
H34	VSS[257]	
F3	VSS[258]	

BD82HM76-SLJ8E-C1_BGA989-D

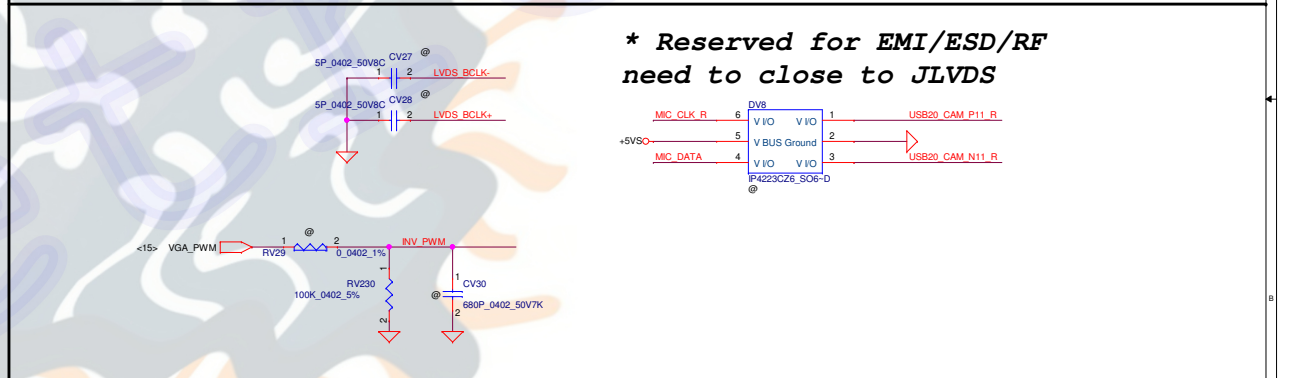
R1@

[illegible]

LCD backlight PWR CTRL



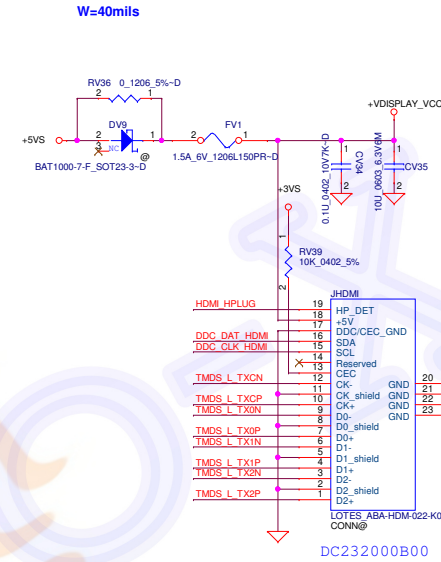
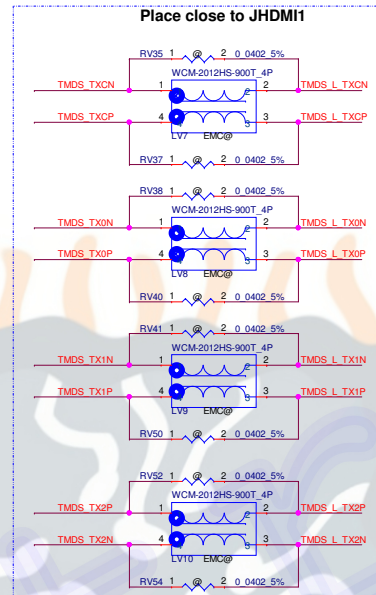
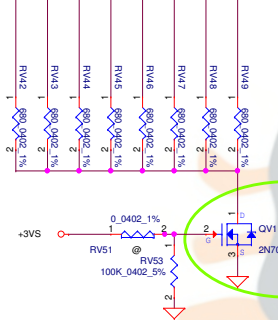
The diagram illustrates a power control circuit for a webcam. It features a +3VS input, a MOSFET (QV8), and various passive components. A green oval highlights the +3VS and +3VS_CAM connection points. The circuit includes resistors RV231, RV34, and RV209, capacitors CV319 and CV31, and a MOSFET QV8. The MOSFET's gate is controlled by a signal labeled <40> CMOS_ON#. The MOSFET's source is connected to ground, and its drain is connected to the +3VS_CAM output.



*** Reserved for LCD sequence tuning**

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/08/22	Deciphered Date	2013/08/31	Title	LVDS/webcam
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT BECAUSE AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-9101P
				Date:	Wednesday, August 29, 2012
				Sheet	21 of 57

<15>	HDMI_A3N_VGA	CV32	2	1	0.1U	0402	10V7K-D	TMDS TXCN
<15>	HDMI_A3P_VGA	CV33	2	1	0.1U	0402	10V7K-D	TMDS TXCP
<15>	HDMI_A0N_VGA	CV36	2	1	0.1U	0402	10V7K-D	TMDS TXCN
<15>	HDMI_A0P_VGA	CV37	2	1	0.1U	0402	10V7K-D	TMDS TXCP
<15>	HDMI_A1N_VGA	CV38	2	1	0.1U	0402	10V7K-D	TMDS TXCN
<15>	HDMI_A1P_VGA	CV39	2	1	0.1U	0402	10V7K-D	TMDS TXCP
<15>	HDMI_A2N_VGA	CV40	2	1	0.1U	0402	10V7K-D	TMDS TXCN
<15>	HDMI_A2P_VGA	CV41	2	1	0.1U	0402	10V7K-D	TMDS TXCP

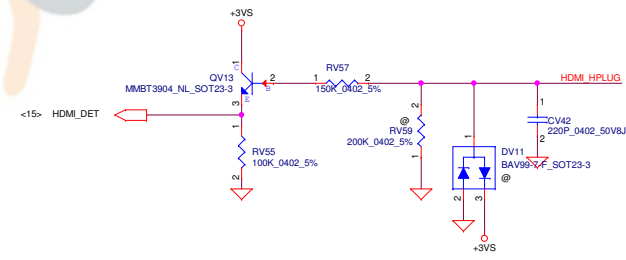
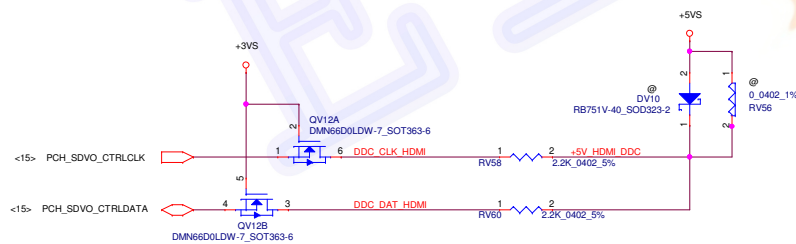


TMDS TXCN	@CV358	1	2	100P	0402	50V8J
TMDS TXCP	@CV360	1	2	100P	0402	50V8J
TMDS TXCN	@CV362	1	2	100P	0402	50V8J
TMDS TXCP	@CV363	1	2	100P	0402	50V8J
TMDS TXCN	@CV359	1	2	100P	0402	50V8J
TMDS TXCP	@CV357	1	2	100P	0402	50V8J
TMDS TXCN	@CV361	1	2	100P	0402	50V8J
TMDS TXCP	@CV364	1	2	100P	0402	50V8J

20111024 EMI ADD

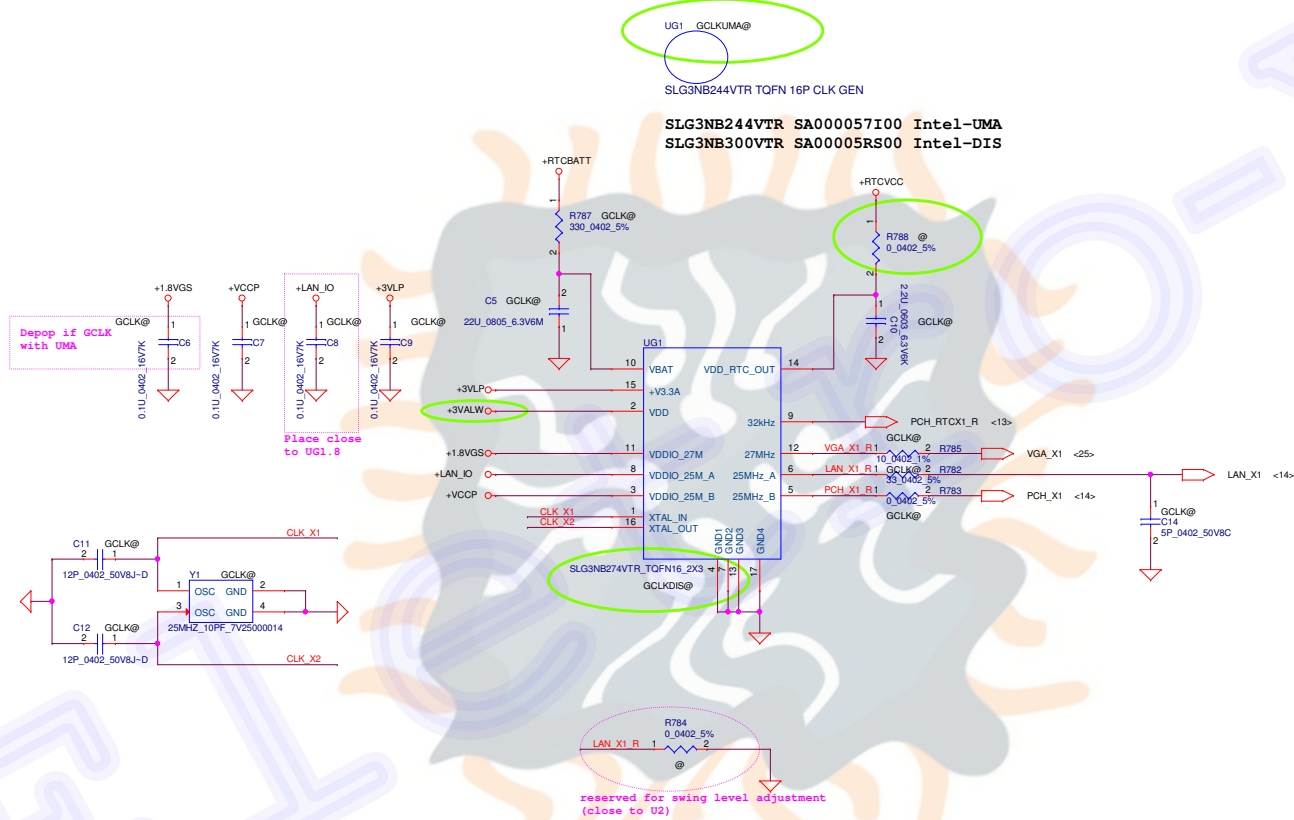
TMDS L TXCN	CV349	1	2	3.3P	0402	50V8C-D
TMDS L TXCP	CV350	1	2	3.3P	0402	50V8C-D
TMDS L TXCN	CV351	1	2	3.3P	0402	50V8C-D
TMDS L TXCP	CV352	1	2	3.3P	0402	50V8C-D
TMDS L TXCN	CV353	1	2	3.3P	0402	50V8C-D
TMDS L TXCP	CV354	1	2	3.3P	0402	50V8C-D
TMDS L TXCN	CV355	1	2	3.3P	0402	50V8C-D
TMDS L TXCP	CV356	1	2	3.3P	0402	50V8C-D

20110805 EMI ADD

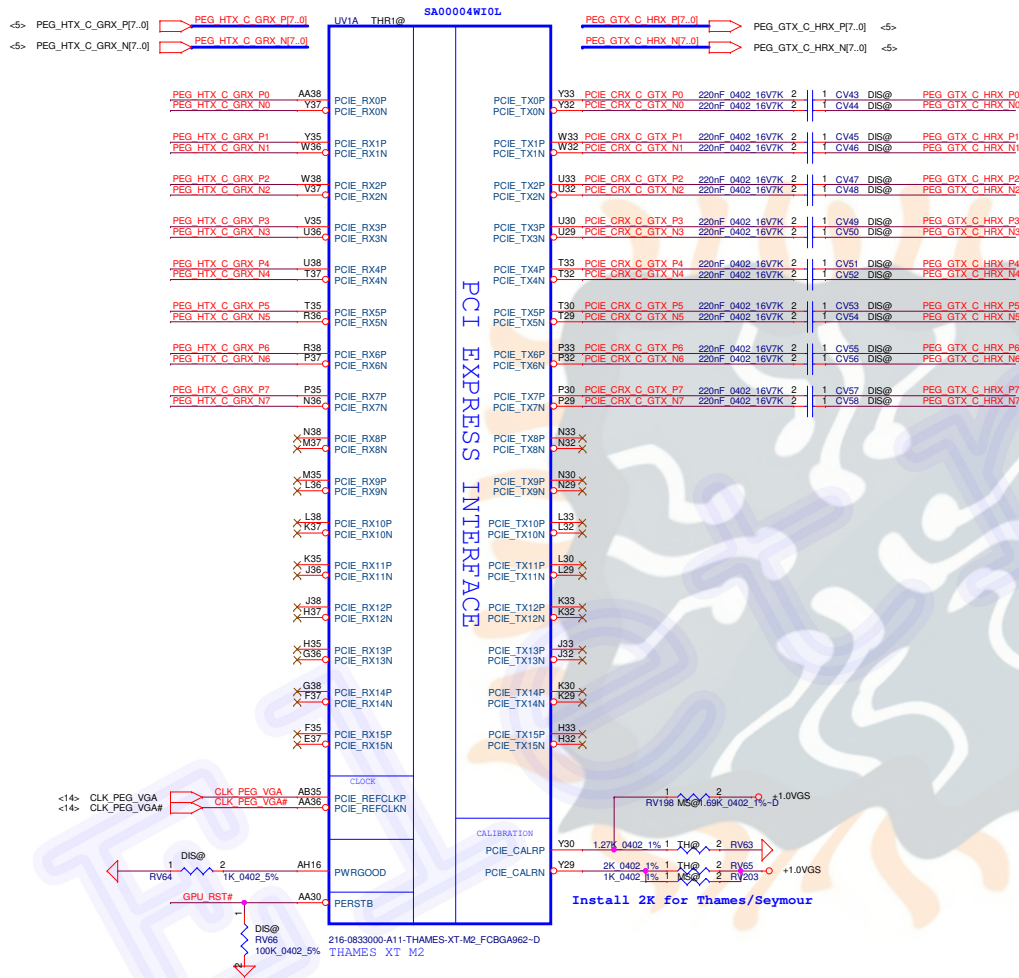


Part Number	Description
8000000023M	HDMI W/Logo:R000000000

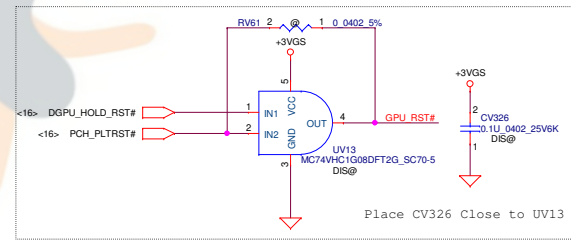
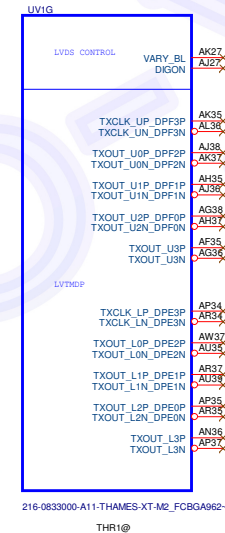
Security Classification	Compal Secret Data	Title	HDMI
Issued Date	2012/08/22	Deciphered Date	2013/08/31
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Document Number	LA-9101P
		Date	Wednesday, August 28, 2012
		Sheet	22
		of	57

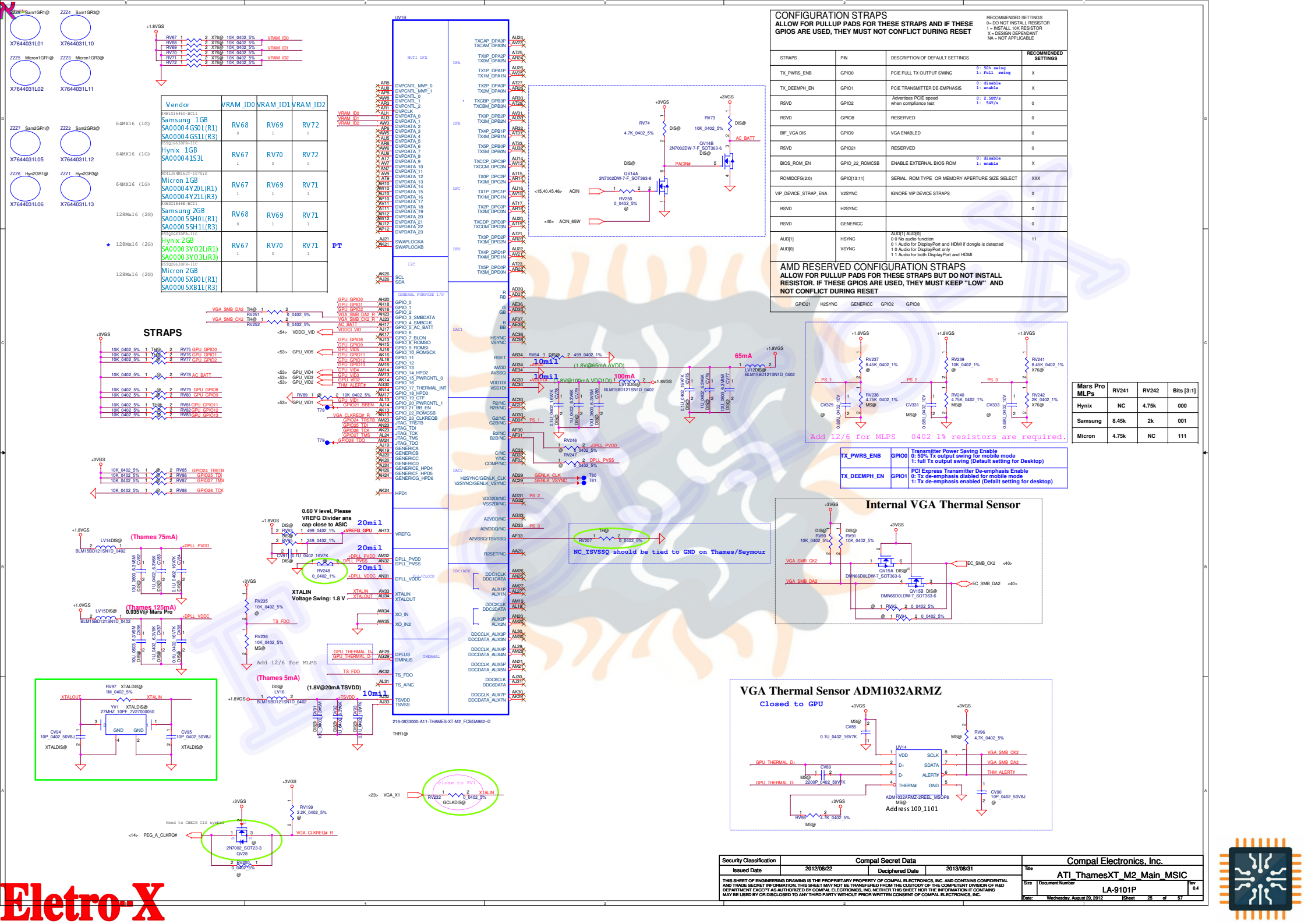


GFX PCIE LANE REVERSAL



LVDS Interface

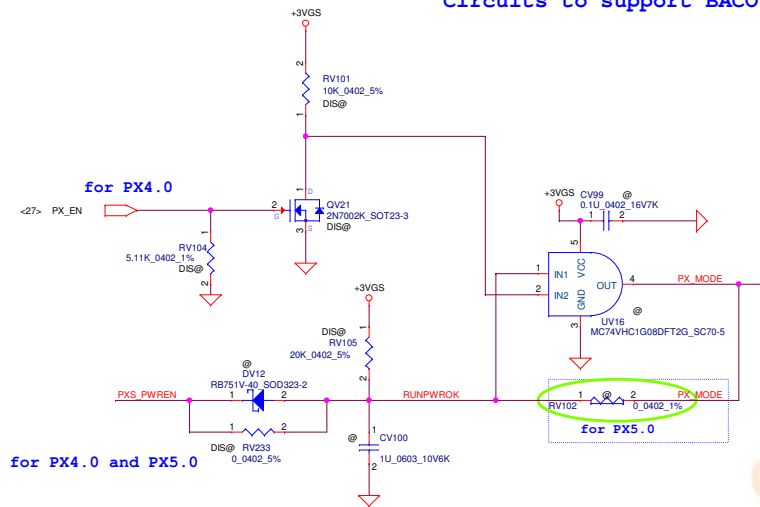




Circuits to support BACO

Switch circuits in BACO designs for Thames/Seymour only

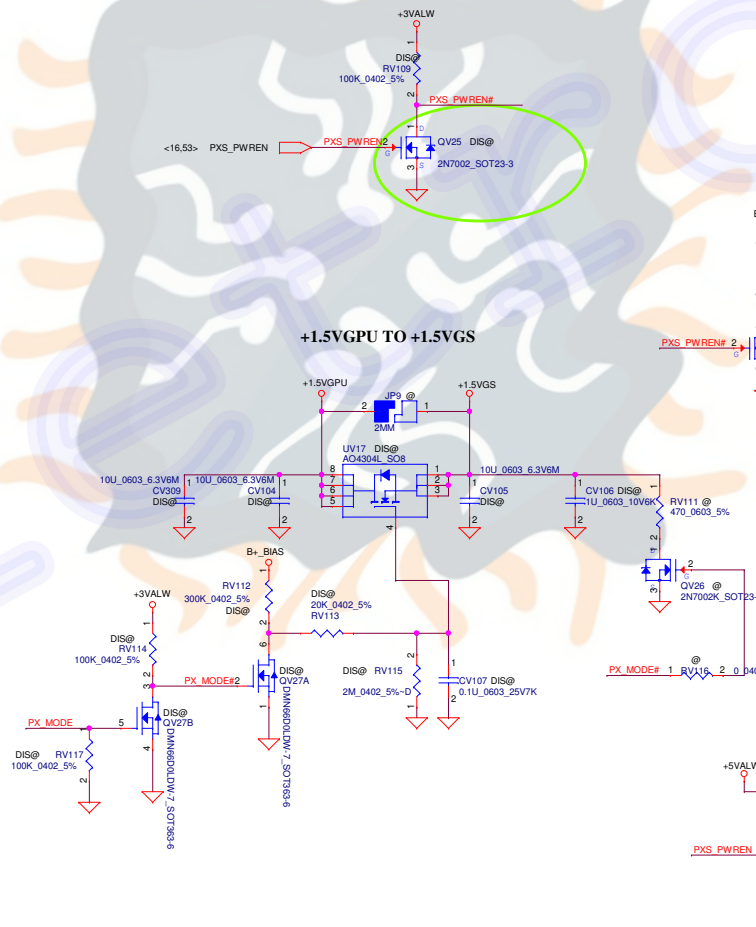
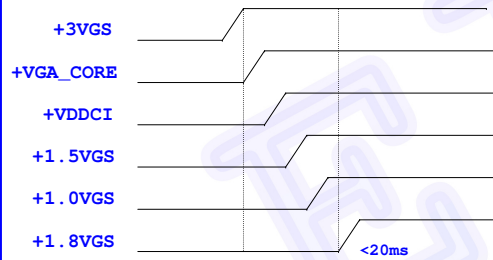
55mA@1.0V, in BACO mode



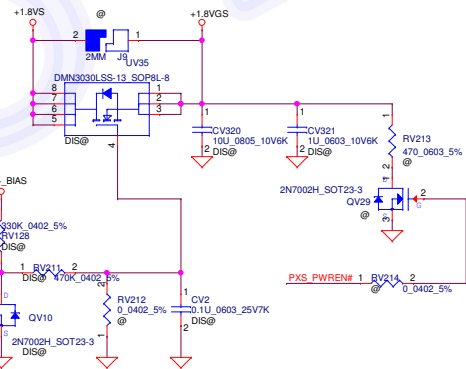
Note:

PX4.0 +VGA_CORE, VDDCI, +1.5VGS ON
 PX4.0 +3VGS, +1.0VGS, +1.8VGS OFF
 PX5.0 +3VGS, +VGA_CORE, VDDCI, +1.5VGS, +1.0VGS, +1.8VGS OFF

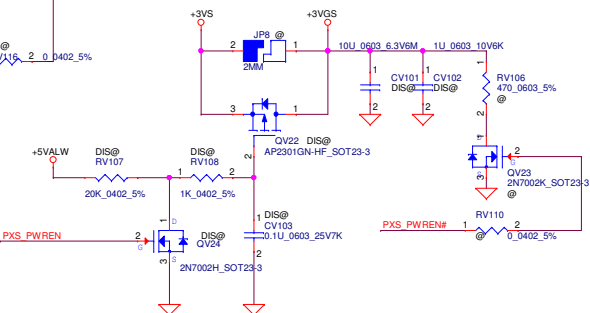
Power Sequence of Thames and Mars Pro

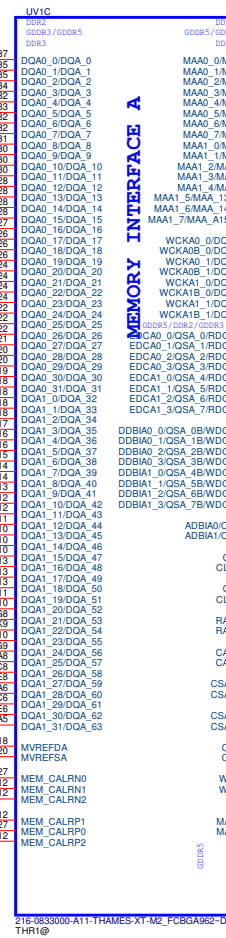


+1.8VS TO +1.8VGS

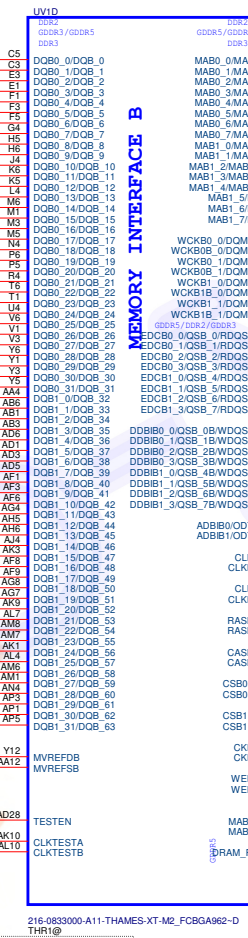


+3.3VS TO +3.3VGS

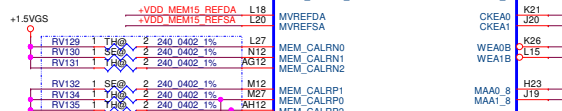




MEMORY INTERFACE A



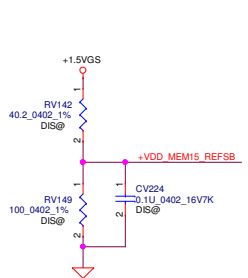
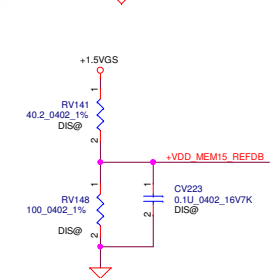
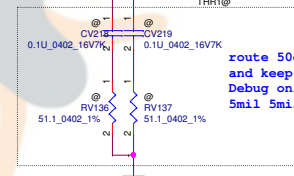
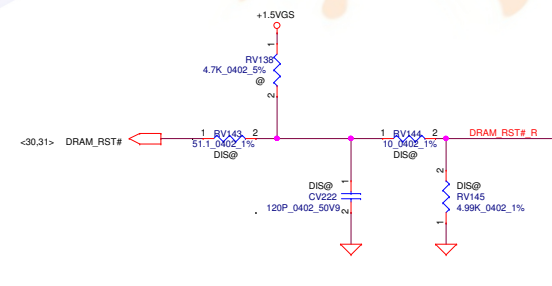
MEMORY INTERFACE B



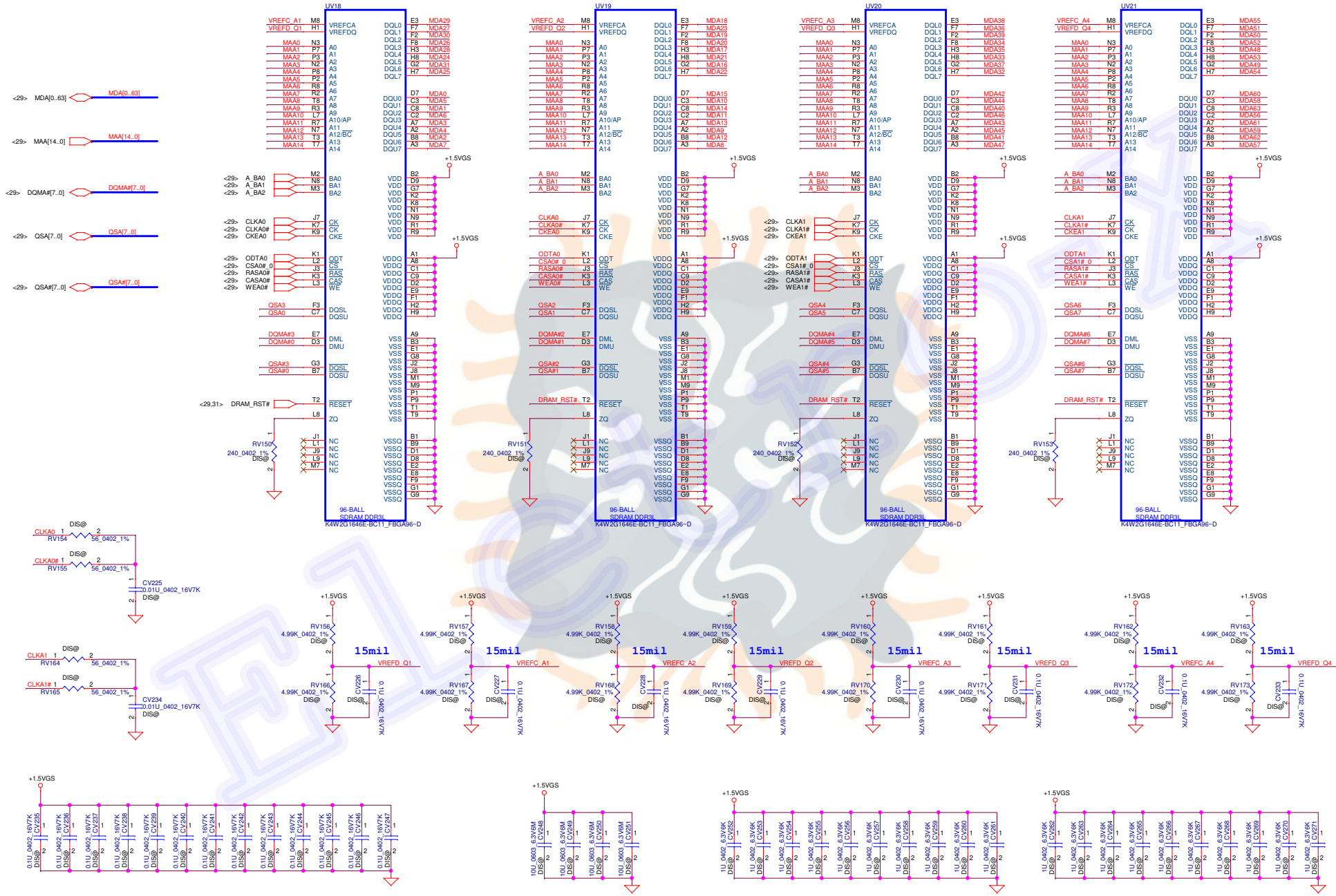
Co-Lay Thames/Seymour/Mars Pro

	Thames M2	Seymour M2	Mars Pro
RV129	TH@	@	@
RV130	@	SE@	@
RV131	TH@	@	@
RV132	@	SE@	@
RV133	TH@	@	@
RV134	TH@	@	@
RV135	TH@	@	@
RV206	@	@	MS@
RV205	@	@	@

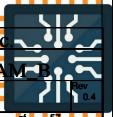
This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and I Cap values will depend on the DRAM load and will have to be calculated for different Memory, DRAM load and board to pass Reset Signal Spec. Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2



CHANNEL A: 256MB/512MB DDR3



Eletro-X



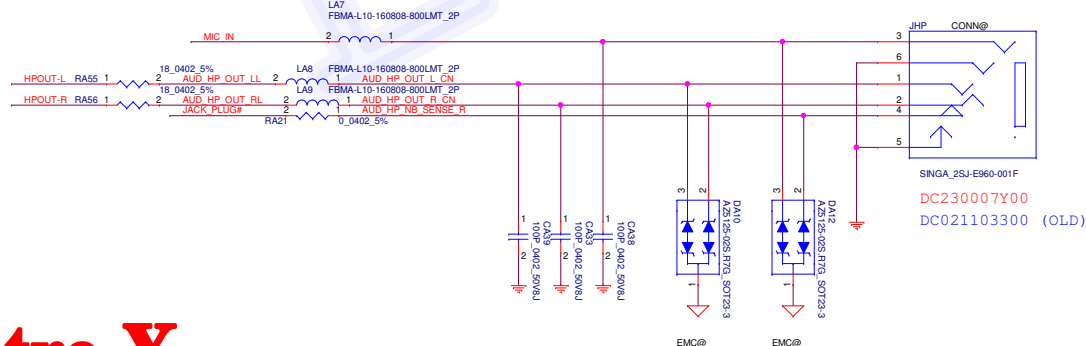
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/08/22	Deciphered Date	2013/08/31	Title	ATI ThamesXT M2 VRA
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
					LA-910IP
Date:		Wednesday, August 29, 2012		Sheet	31

CA59, CA60
Close to UA1
Pin36

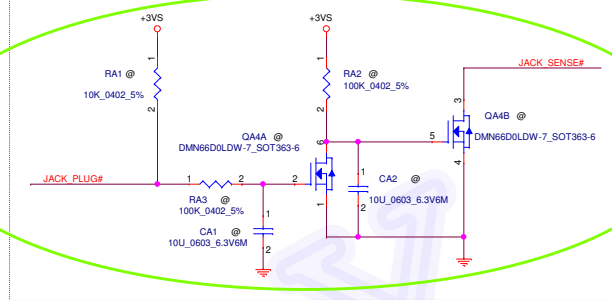
HDA_RST_AUDIO#
0.1U_0402_16V7K
Place close to UA1.11

HDA BITCLK AUDIO
22P_0402_50V8J

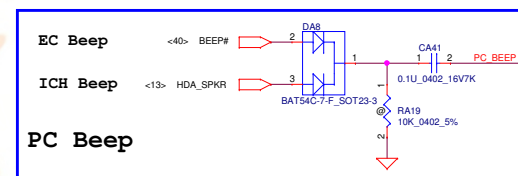
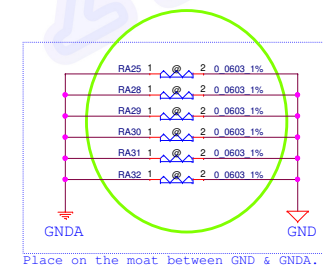
iPhone type Combo Jack



JACK_PLUG Delay circuit

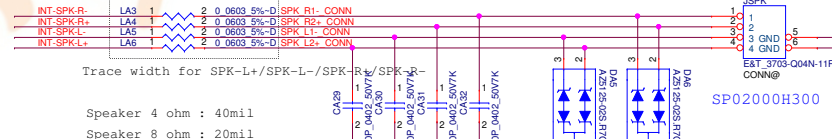


JACK_PLUG# RA4 1 2 0.0402_5% JACK_SENSE#
Reserve for cancel Delay circuit

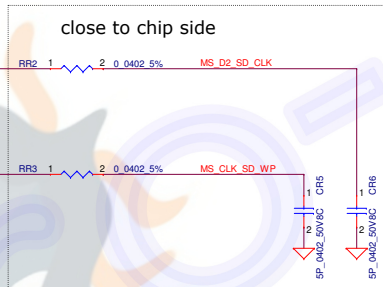
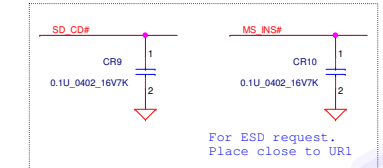
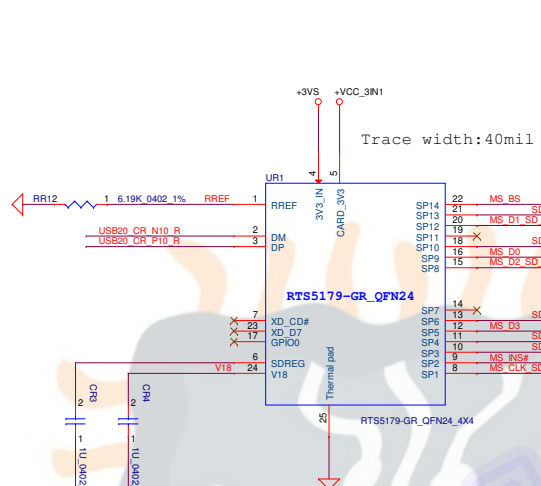
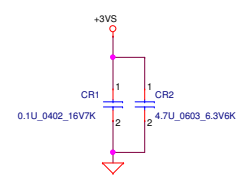
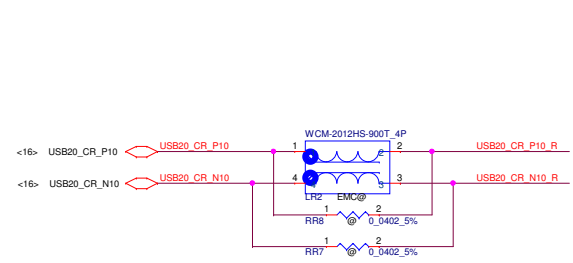


Close to UA1
Pin11,13,14,16

close to Codec

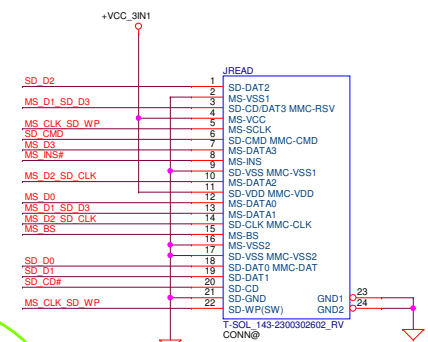
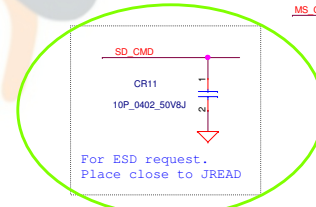
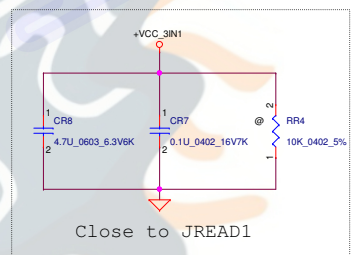


Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil



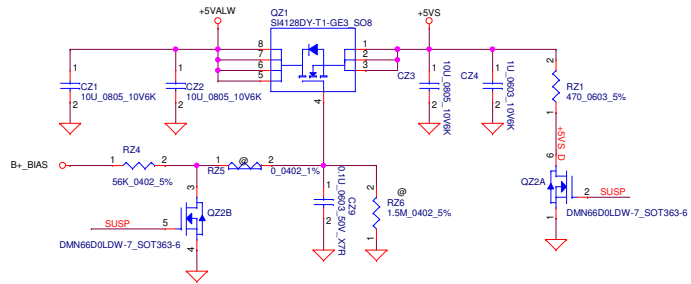
拉MS_D2_SD_CLK到Conn pin 13 SD_CLK
再打Via拉到pin 10 MS_D2

拉MS_CLK_SD_WP到Conn pin 5 MS_CLK
再打Via拉到pin 20 SD_W

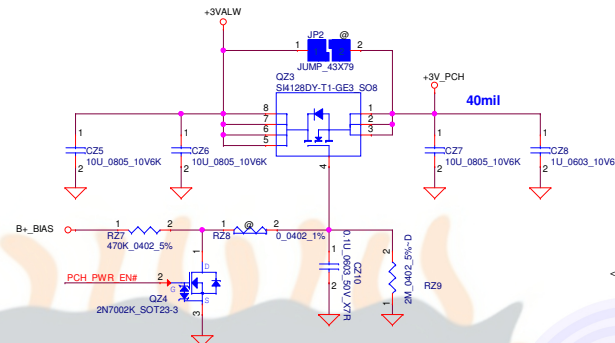


SP071204100
LTCX004AK00

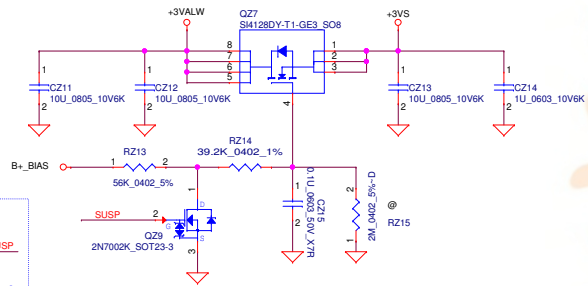
+5VALW to +5VS



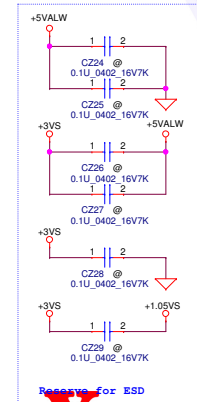
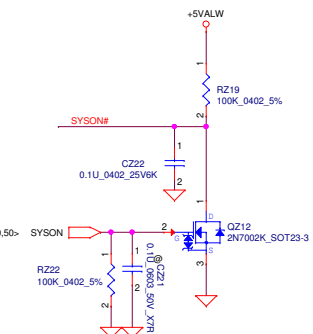
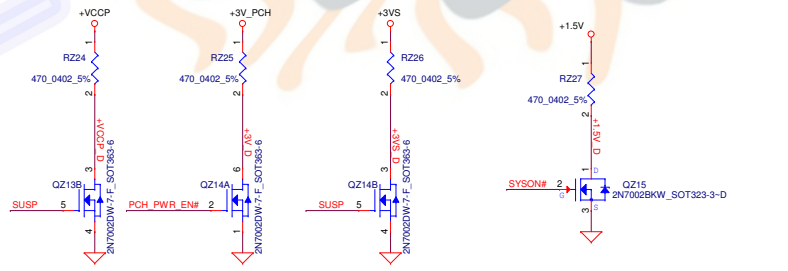
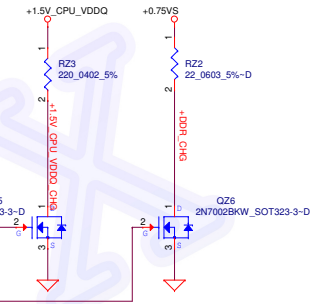
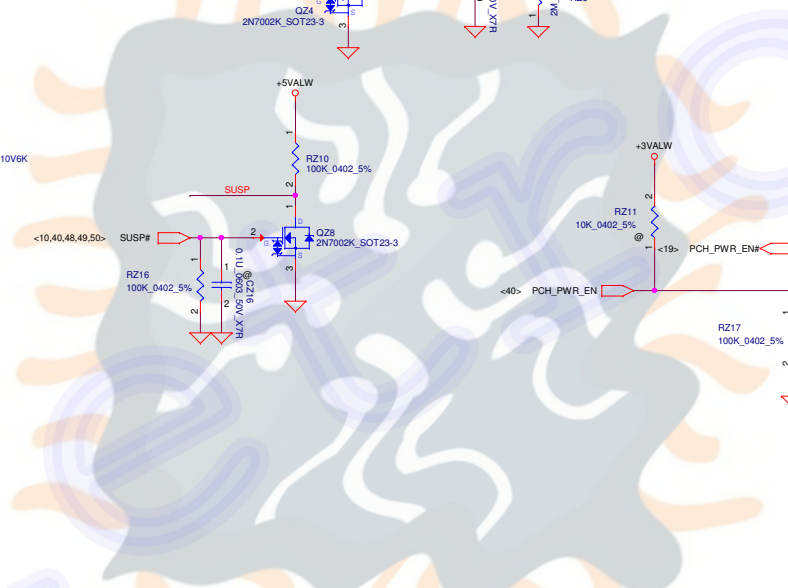
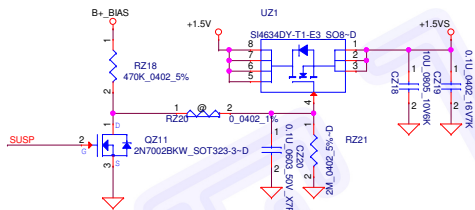
+3VALW to +3V_PCH

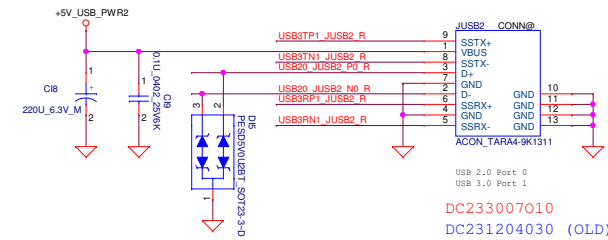
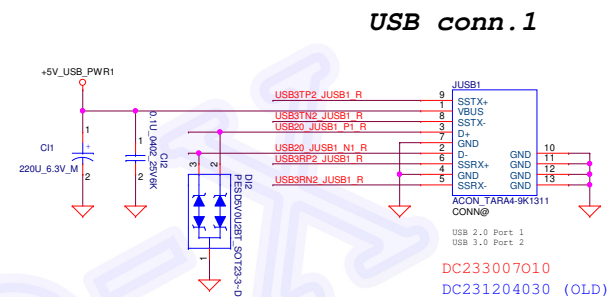


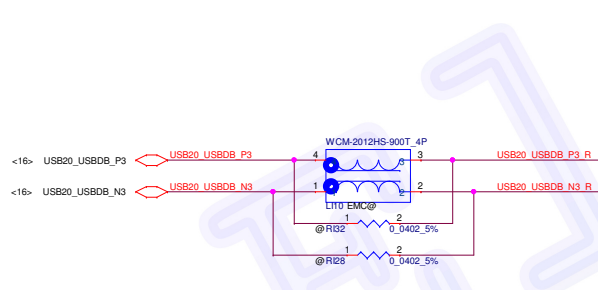
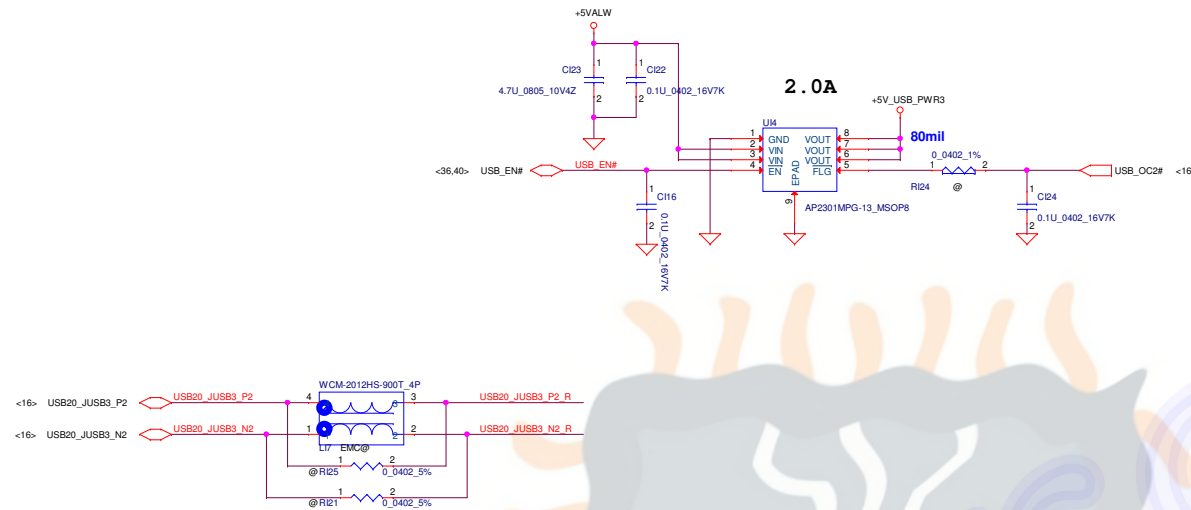
+3VALW to +3VS



+1.5V To +1.5VS







Eletro-X

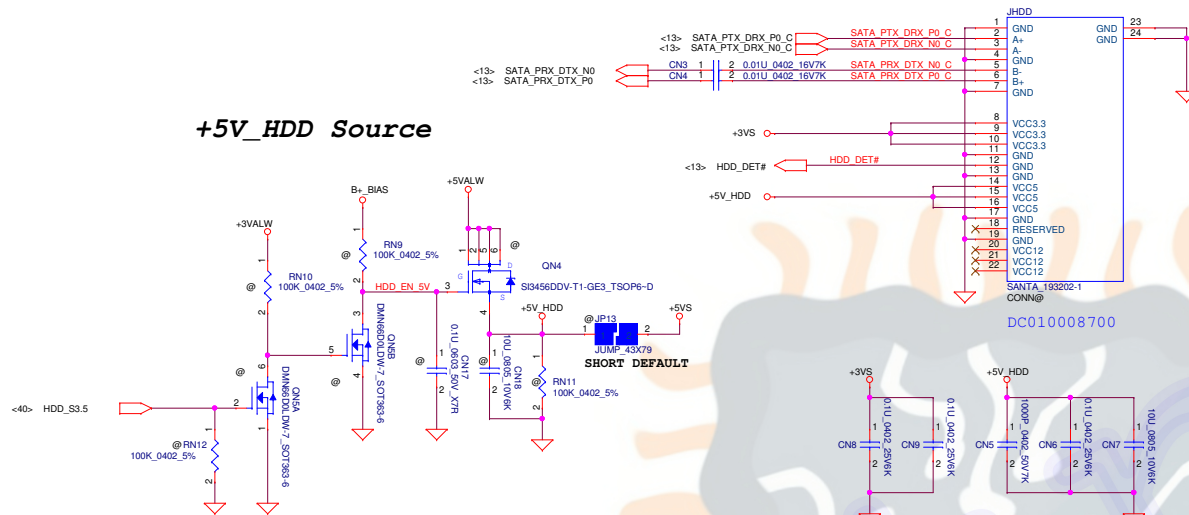


ON/OFF switch

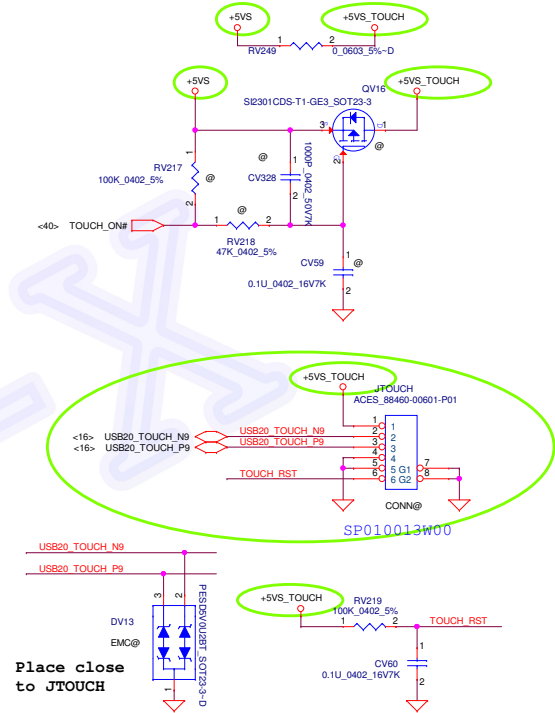


SATA HDD Conn.

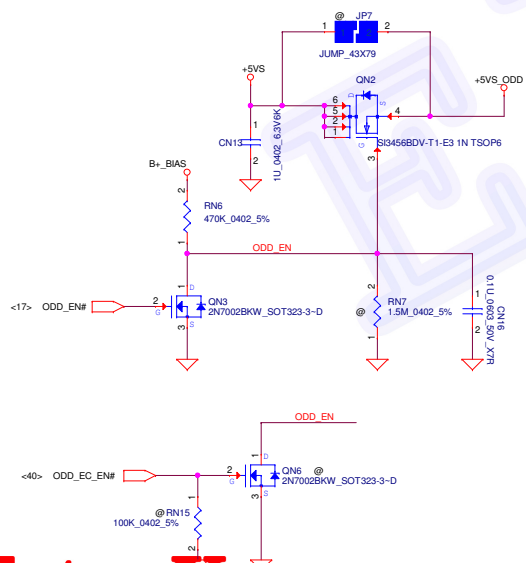
+5V_HDD Source



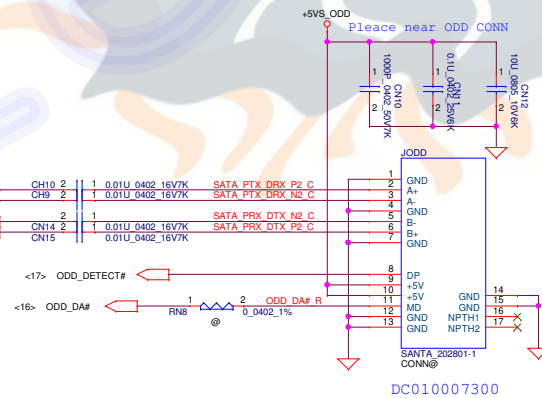
* Touch Screen Panel

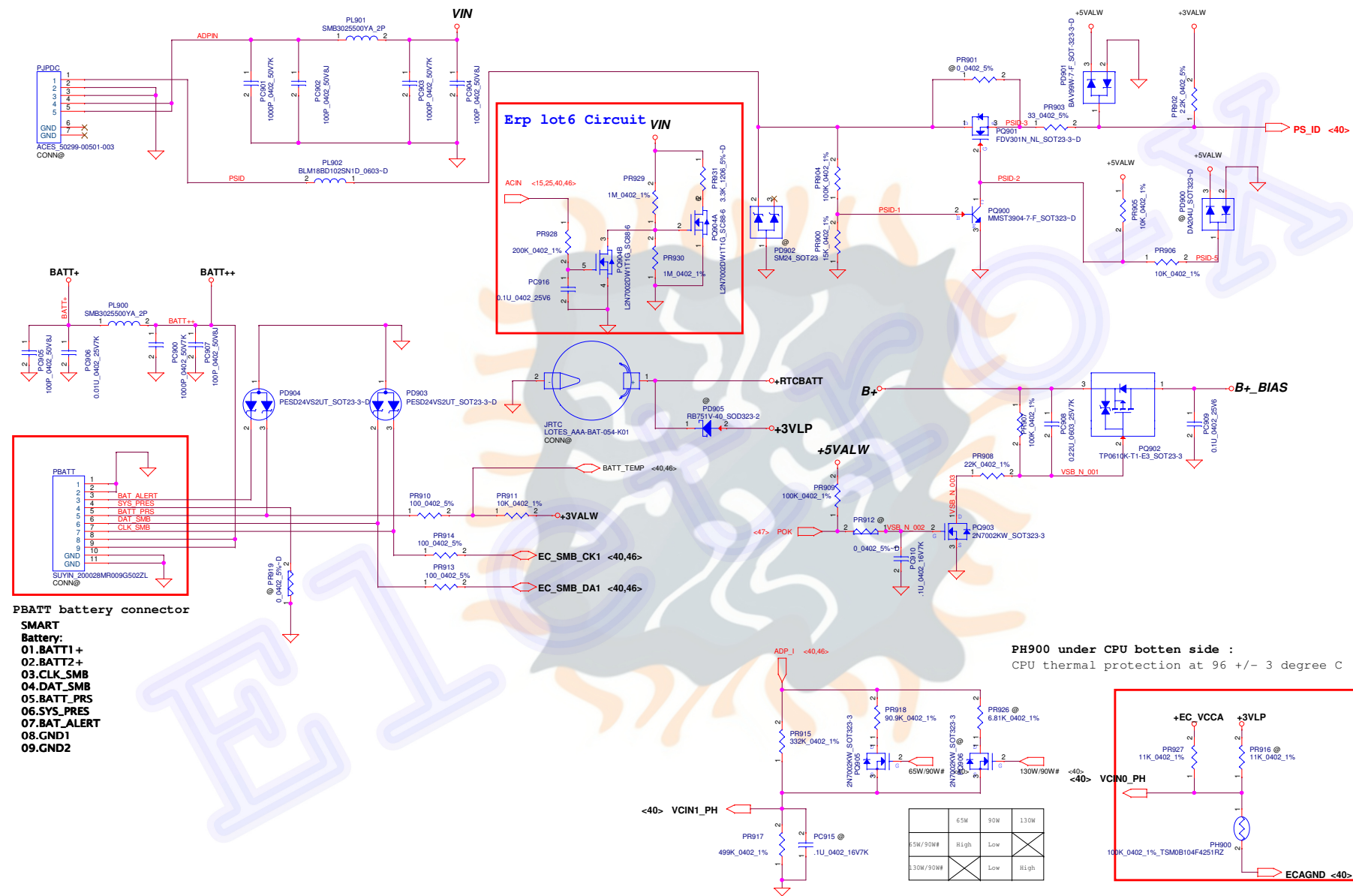


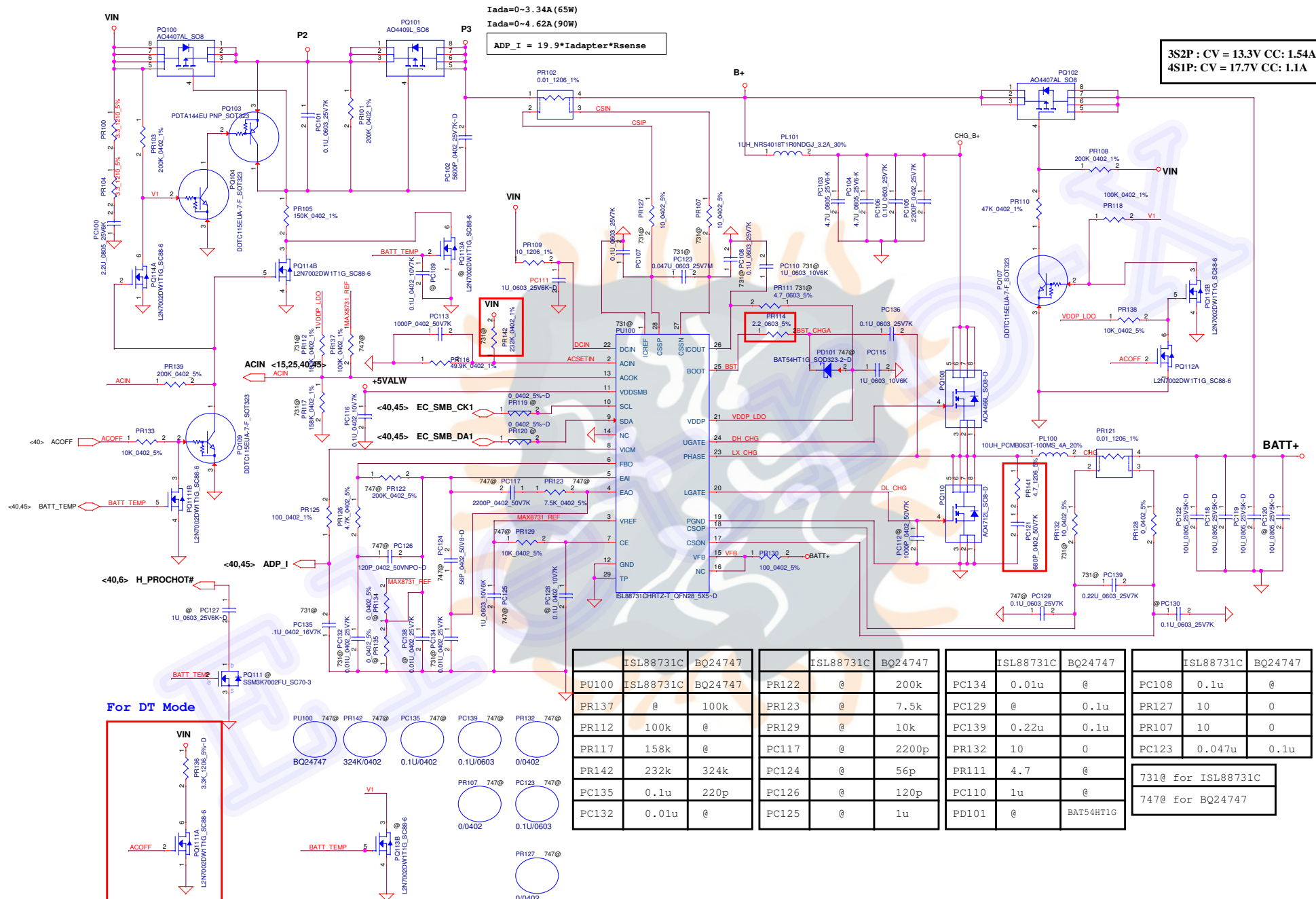
ODD Power Control



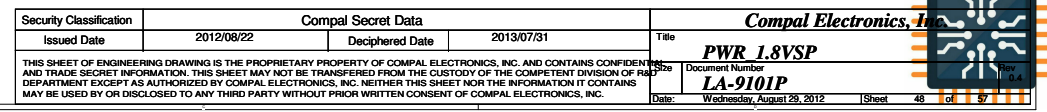
SATA ODD Conn.

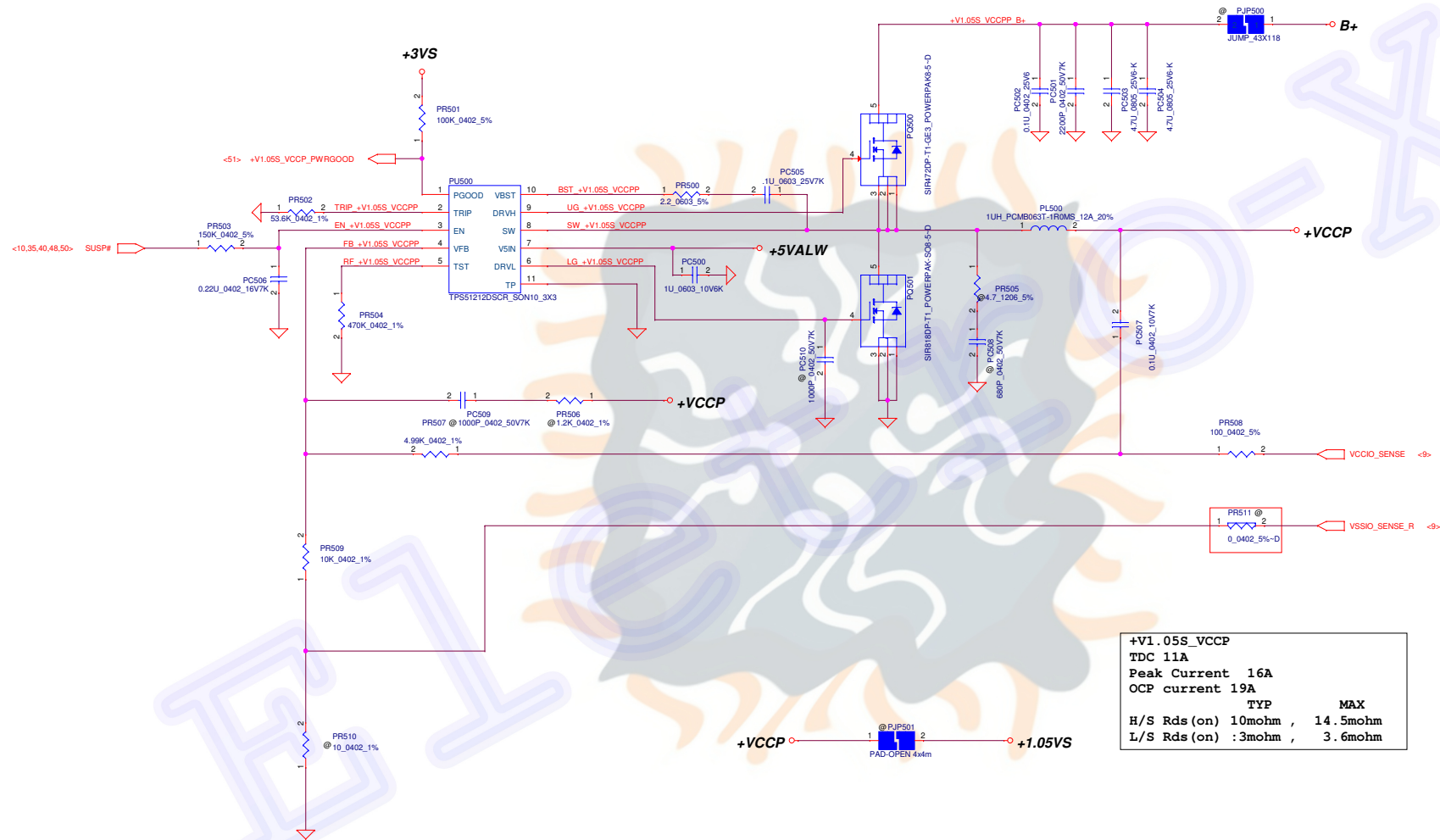






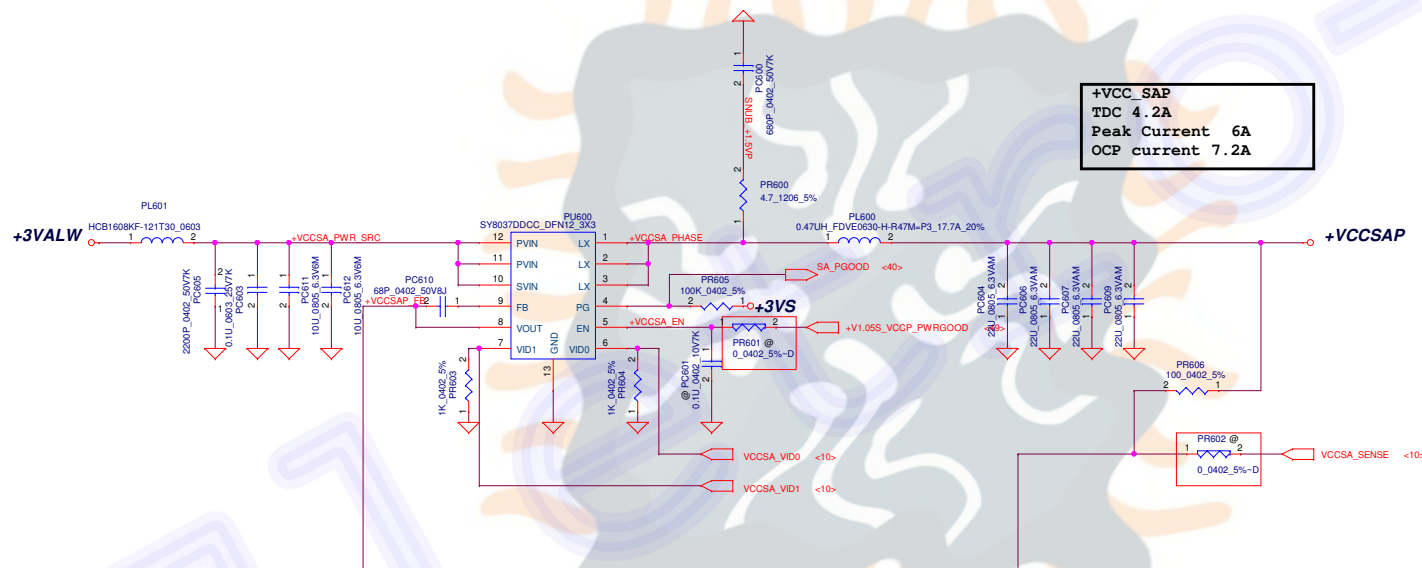
	ISL88731C	BQ24747		ISL88731C	BQ24747		ISL88731C	BQ24747		ISL88731C	BQ24747
PU100	ISL88731C	BQ24747	PR122	@	200k	PC134	0.01u	@	PC108	0.1u	@
PR137	@	100k	PR123	@	7.5k	PC129	@	0.1u	PR127	10	0
PR112	100k	@	PR129	@	10k	PC139	0.22u	0.1u	PR107	10	0
PR117	158k	@	PC117	@	2200p	PR132	10	0	PC123	0.047u	0.1u
PR142	232k	324k	PC124	@	56p	PR111	4.7	@	731@ for ISL88731C		
PC135	0.1u	220p	PC126	@	120p	PC110	1u	@	747@ for BQ24747		
PC132	0.01u	@	PC125	@	1u	PD101	@	BAT54HT1G			



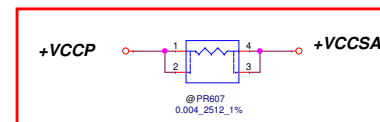


VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

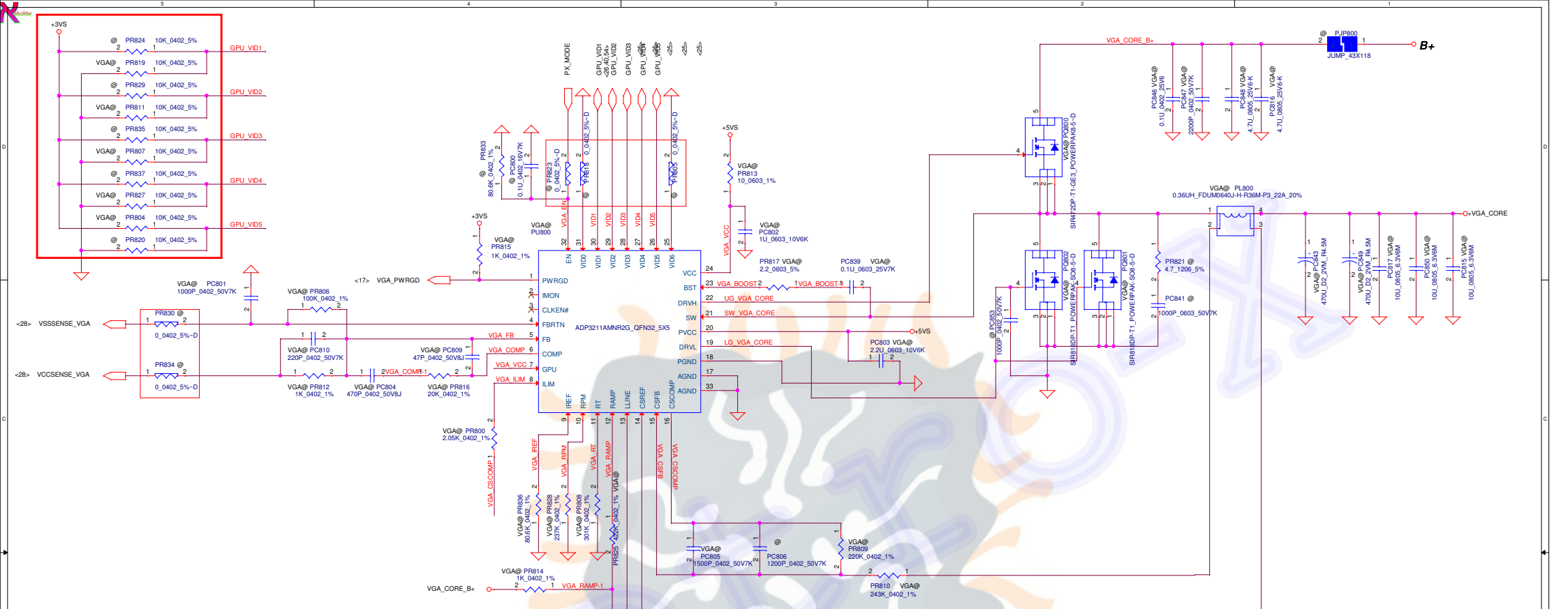
output voltage adjustable network



The 1k PD on the VCCSA VIDs are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.



reserve for Pentium and Celeron only



Mars Pro

GPU_VID5 (GPIO_10)	GPU_VID4 (GPIO_14)	GPU_VID3 (GPIO_15)	GPU_VID2 (GPIO_16)	GPU_VID1 (GPIO_20)	Core Voltage Level
0	1	1	1	1	1.125V
1	0	0	0	0	1.1V
1	0	0	0	1	1.075V
1	0	0	1	0	1.05V
1	0	0	1	1	1.025V
1	0	1	0	0	1V
1	0	1	0	1	0.975V
1	0	1	1	0	0.95V
1	0	1	1	1	0.925V
1	1	0	0	0	0.9V
1	1	0	0	1	0.875V
1	1	0	1	0	0.85V
1	1	0	1	1	0.825V
1	1	1	0	0	0.8V

+VGA_CORE
TDC 22A
Peak Current 30A
OCP current 36A
FSW=350kHz
DCR 1.1mohm +/-5%
Loadline = 1.5mohm

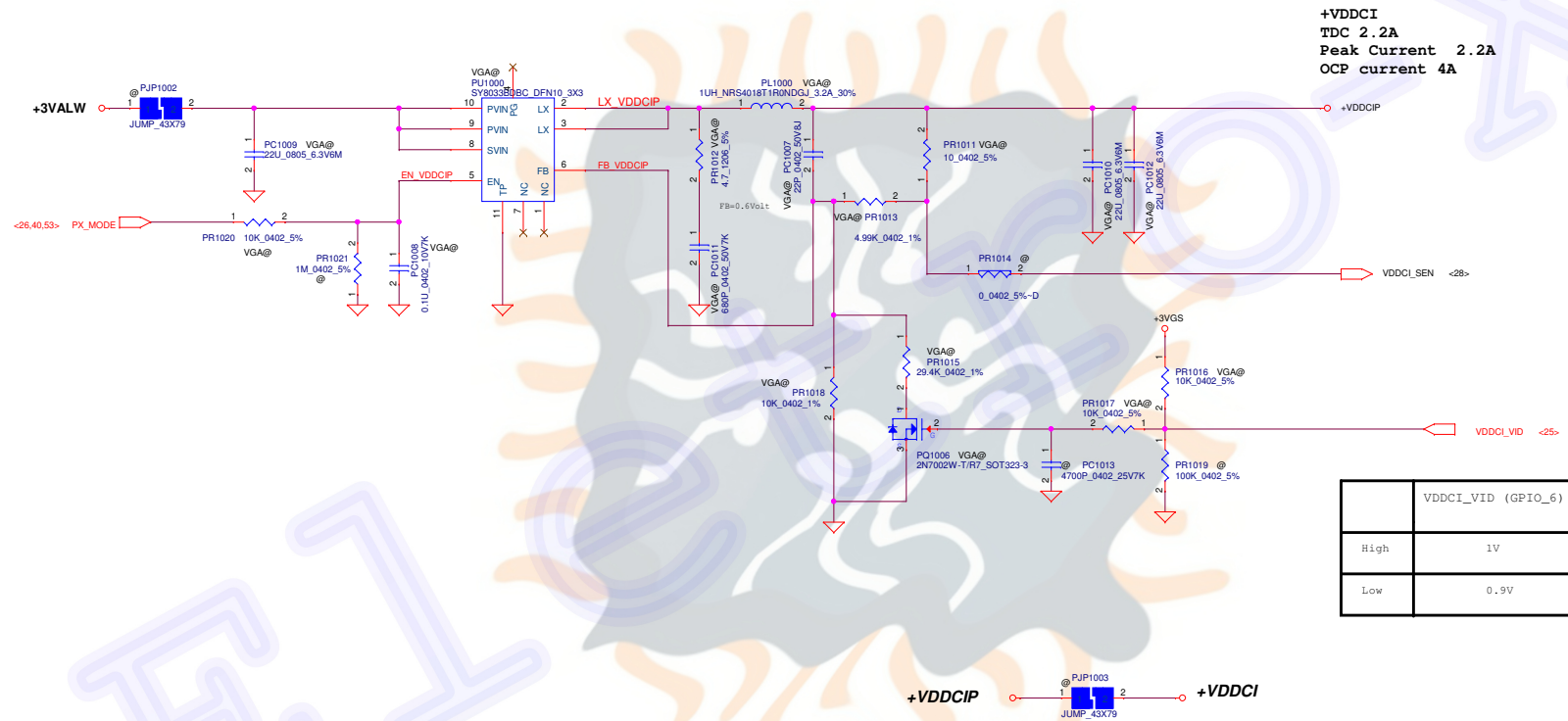
Thames XT

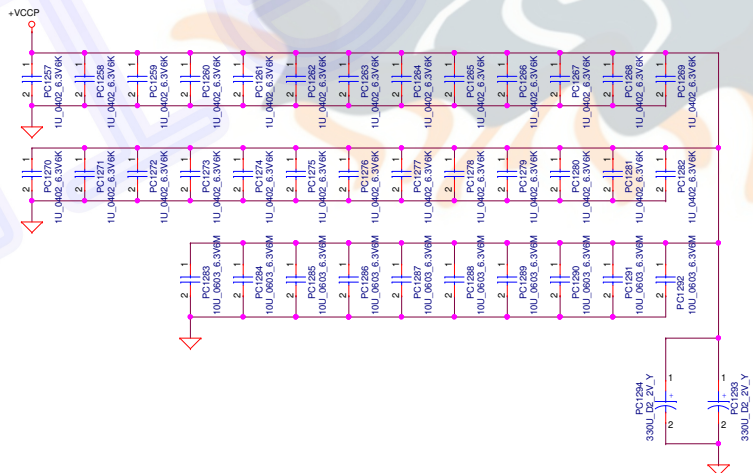
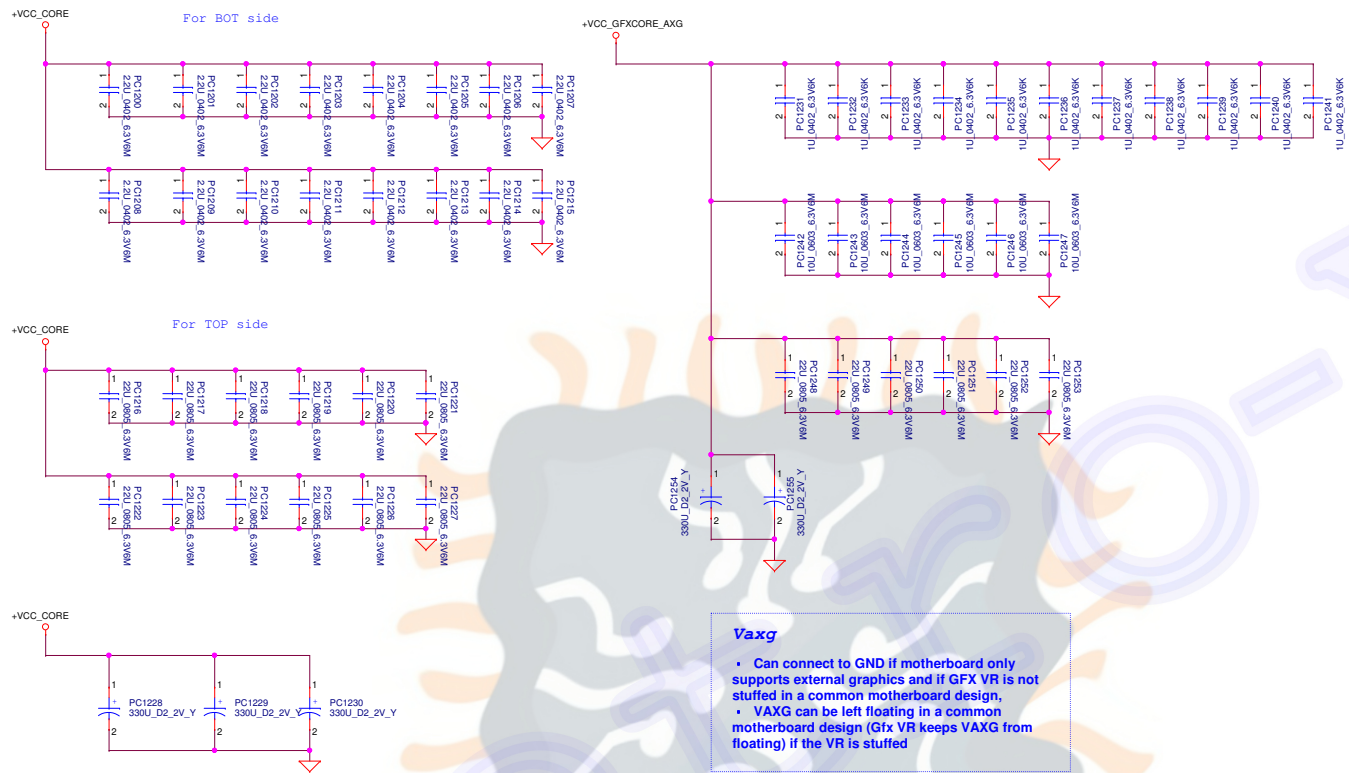
GPU_VID5 (GPIO_10)	GPU_VID4 (GPIO_14)	GPU_VID3 (GPIO_15)	GPU_VID2 (GPIO_16)	GPU_VID1 (GPIO_20)	Core Voltage Level
1	0	0	1	0	1.05V
1	0	1	0	0	1V
1	0	1	1	0	0.95V
1	1	0	0	0	0.9V

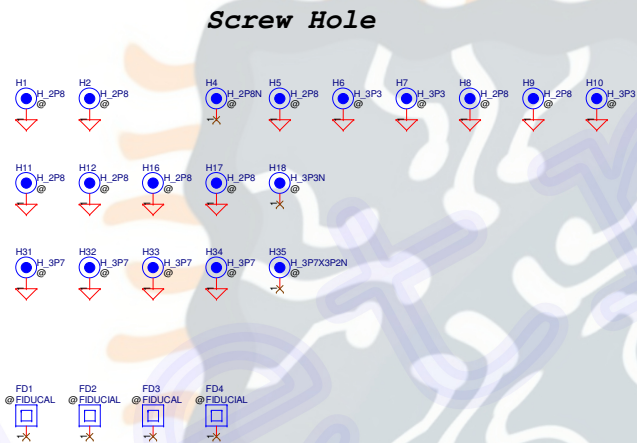
+VGA_CORE
TDC 20A
Peak Current 30A
OCP current 36A
FSW=350kHz
DCR 1.1mohm +/-5%

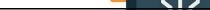
+VGA_PCIE
TDC 3.6A
Peak Current 5.2A
OCP current 6A

	Thames XT	Mars Pro
VGA_PCIE	1.0V	0.95V
PR832	6.81K	5.9K







Security Classification		Compal Secret Data			
Issued Date	2012/08/22	Deciphered Date	2013/07/31	Title	PWR-PIR
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Date Wednesday, August 29, 2012	Sheet 57 of 57
				Date Wednesday, August 29, 2012	Sheet 57 of 57

Version Change List (P. I. R. List)

Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	Card Reader	2012/04/27	HW	The Card reader USB signal is incorrect.	SWAP UR1 USB signal P/N	0.2
2	40	Keyboard	2012/05/03	SED	Keyboard pin define change.	Follow new SPEC.SWAP JKB pin define.	0.2
3	16, 21, 34, 36, 37, 38	USB	2012/05/04	Function team	Change USB port assignment for function team request	USB port change detail please reference Page.16 description.	0.2
4	26	VGA	2012/05/05	HW	Delete reserve BACO circuit	Delete UV15, QV16, QV17, QV18, QV19, QV20, RV99, RV100, RV249, CV96, CV98	0.2
5	42	DC/DC	2012/05/07	HW	Design change	UN-POP R211, POP R217	0.2
6	33	Audio codec	2012/05/09	ESD	ESD team ask solution	Add RA29, RA30, RA31, RA32 and place on the moat between GND & GNDA	0.2
7	6, 17	PCH	2012/05/09	ESD	ESD team ask reserve solution	Add CC151, CH102 for reserve	0.2
8	32	LAN	2012/05/10	HW	Remove China Go-rural for DELL request	Remove DL7, DL8, DL9	0.2
9	16, 38	USB	2012/05/10	HW	Remove JUSB3 USB3.0	Delete LI8, LI9, DI6 and change JUSB3 to USB2.0 type	0.2
10	32	Crystal	2012/05/15	HW	Crystal vendor suggestion	Change CL36, CL37 from 33p/0402 to 12p/0402	0.2
11	21, 39	LVDS	2012/05/17	SED	Add FHD Panel CE_ENABLE, DBC_ENABLE function from SED request	Add CE_EN, DBC_EN control pin to EC	0.2
12	21	LVDS	2012/05/22	SED	Follow SED team request disable CE_EN function	Change RV62 to DE-POP and RV100 to POP for disable CE_EN function	0.2
13	33	Audio codec	2012/05/23	CODEC	Follow CODEC vendor suggestion	Add AUDIO JACK PLUG delay circuit, Spereate NET JACK_PLUG to -> JACK_SENSE# & -> JACK_PLUG#	0.2
14	16, 21	Touch Screen	2012/05/29	HW	Add touch screen function	Add RV217, RV218, RV219, RV249, CV59, CV60, CV328, DV13, QV16, JTOUCH	0.2
15	39	Board ID	2012/05/30	HW	Board ID change for PT	Change RE5 from 8.2k_0402(SD028820180) to 33k_0402(SD028330280)	0.2
16	21, 39	Touch Screen	2012/05/30	HW	Add touch screen function power control	Add NET "TOUCH_ON#" from JTOUCH to UE1.82(KB9012) for TOUCH SCREEN PANEL power control	0.2
17	33	Audio codec	2012/05/30	HW	Follow RealTek suggestion remove, delete reserve MUTE circuit	Delete D1, QA1, QA2, QA3, RA24, RA26, RA60, RA62, RA68, RA109, CA72, CA73	0.2
18	15, 16, 39, 41	ESD	2012/05/30	ESD	ESD ask CAP for reserve	Reserve 0.1u/0402 CH104, C223, CH105, CE27, CE28	0.2
19	14	Green CLK	2012/05/30	HW	For Green CLK test	Change RH31, RH41, RV232 0ohm form "GCLK#" to "g" for break the clock signal to device	0.2
20	10, 26, 41	DC/DC	2012/05/31	HW	Change "+1.5V_CPU_VDDQ", "+1.5VS", "+1.5VGS" derating	Change RC150 330K/0402 to 2M/0402, RC151 100K/0402 to 470K/0402, R218 100K/0402 to 470K/0402, RV115 0/0402 to 2M/0402	0.2
21	41	DC/DC	2012/05/31	HW	For power sequence trunning	Change R215 to DE-POP	0.2
22	06, 15, 16, 39, 41	ESD	2012/05/31	ESD	Follow ESD team request	Change 0.1u/0402 from "g" to POP	0.2
23	32	Green CLK	2012/06/15	HW	Change for Green CLK bom control	Change RL21, RL30 from "g" to "GCLK#"	0.2
24	41	DC/DC	2012/06/15	HW	For WLAN card power sequence issue	Change R24, R213 from 470K/0402 56K/0402	0.2
25	35, 41	Schematic page modify	2012/06/18	HW	Schematic page modify for easily maintain.	Swap Page. 35 & Page 41.	0.2
26	41	ODD	2012/06/18	HW	Change component location for easily maintain.	Move RH42, RH43 from Page.13 to Page.41.	0.2
27	39	FAN	2012/06/29	HW	Fan speed noise issue	Reserve 220p/0402 CE24	0.3
28	6	CPU	2012/06/29	ESD	System boot-up shot down issue.	Change CC151 from POP to "g"	0.3
29	21, 35, 39, 40, 41	Circuit adjust	2012/07/01	HW	Circuit & page adjust for OAK 15" & OAK 17"	1. Swap P.35 & P.41and move touch screen circuit from P.21 to P.41. 2. Swap P.39 & P.40 page no	0.3
30	40	LID SW	2012/07/01	HW	LID SW need a trace for debug and switch.	Add RE81 for LID SW.	0.3
31	25	GPU	2012/07/01	HW	Follow AMD request, MarsPro will used MPLs.	Change RV75, RV76, RV81 from "DIS#" to "TH#"	0.3
32	29	GPU	2012/07/01	HW	Follow AMD request, MEM_CALRP2 is not need for Mars ASIC now.	Change RV205 from "MS#" to "g"	0.3
33	38	MINI card	2012/07/03	HW	Power Control for Mini card didn't need	Change R17 to "g"	0.3
34	6	XDP	2012/07/06	HW	S3 return hang issue	Change RC89 from "g" to POP	0.3
35	23	GREEN CLK	2012/07/09	HW	Follow Green CLK FAE suggestion	1. Change UG1.2(+3VLP) & UG1.8(+3VALN) connect to +LAN_IO 2. Add R787 connect from +RTCBATT to C5.2 & UG1.10 3. Change C14 from 0.1u to 5p/0402 4. Change C8 connect from +3V_ALW to +LAN_IO 5. Add R788 0ohm/0402 from +RTCVCC to UG1 for GCLK & DH1 select	0.3
36	35	MOAT	2012/07/09	ESD	For ESD request reserve CAP.	Reserve those CAP for ESD MOAT.	0.3
37	18	LVDS	2012/07/10	HW	Change RES and reserve CAP for LVDS issue	Change RH185 from 0ohm-short to 0ohm/0805, and reserve CH106 1U/0402	0.3
38	41	Connector	2012/07/10	ME	For ME request	Change JBTB1 footprint from SP02000G800 (OLD) to SP02000MJ00	0.3
39	13	PCH	2012/07/11	ESD	Follow ESD team request	Add RH44, RH48, RH70 & NET PCH_JTAG_TMS_R, PCH_JTAG_TDI_R, PCH_JTAG_IDO_R for break signal trace	0.3
40	40	PCH	2012/07/11	ESD	Follow ESD team request	1. Change NET NAME "N59110727" to "WL_BT_LED#_R" 2. Reserve 0.1u/0402 on "WL_BT_LED#_R" for ESD	0.3
41	21	LVDS	2012/07/11	HW	Reserve for CE function for LVDS connector	Change CE_EN_R from dummy to JLVDS.18	0.3

Security Classification	Compal Secret Data		Title HW-PIR Document Number LA-9101P Date: Wednesday, August 28, 2012 Sheet 43 of 57
Issued Date	2012/08/22	Deciphered Date	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
40	32	Connector	2012/07/12	ME	For ME request	Change JLAN CPN from "DC234004V00" to "SP011207090"	0.3
41	40	FAN	2012/07/16	HW	For FAN_SPEED1 noise issue	Change CE29 from "@" to POP	0.3
42	14	Touch PAD	2012/07/17	SED	Change Touch PAD SMBUS port for SMBUS issue	Change Touch PAD SMBUS port for SMB0 to SMB	0.4
43	32	GREEN CLK	2012/07/19	HW	Follow Silago FAE request	Change RL21 from 510 ohm to 0 ohm/0402	0.4
44	41	Touch Screen	2012/08/07	SED	Follow SED team request change JTOUCH USB signal conatct.	Change JTOUCH Pin define.	0.4
45	34	Card Reader	2012/08/14	ESD	Follow ESD team request	Reserve CR11 100p/0402 close to JREAD	0.4
46	23	GREEN CLK	2012/08/16	HW	Fixed GCLK output abnormal issue	Change UG1.2(UG1/VDD) from +LAN_IO to+3VALW	0.4
47	33	CODEC	2012/08/16	HW	The issue already fixed by new CODEC.	Remove delay circuit and POP RA4	0.4
48	23	GREEN CLK	2012/08/17	HW	For RTC discharge issue	De-pop R788	0.4
49	32,34	LAN	2012/08/17	HW	For LAN Chip abnormal leakage issue	Pop RL34 and de-pop RE21	0.4
50	34	Card Reader	2012/08/20	ESD	Follow ESD team request	Change CR11 from 100p/0402 to 10p/0402 and POP	0.4
51	41	Touch Screen	2012/08/20	SED	Follow SED team request	Change Touch screen power rail for +3VS to +5VS	0.4
52	38	LED	2012/08/20	HW	Change LED light	Change LED1,LED2,LED4 CPN from SC500006000 to SC50000DC00	0.4
53	38	WLAN	2012/08/20	HW	Remove AGAC function power control	Change R18,R19,R20,R21,C13,Q2,Q4 component BOM structure to "@"	0.4
54	41	Touch Screen	2012/08/20	HW	Add EC control for Touch Screen function	Add RN15 & QN6 and relative circuit connect	0.4